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## ABSTRACT

### INFLUENCE OF $\text{SiN}_x/\text{Si}$ INTERFACE STATES ON Si SOLAR CELLS

by  
Santosh Sahoo

Impact of the  $\text{SiN}_x/\text{n}^+\text{-Si}$  interface on silicon solar cell performance was investigated, where  $\text{SiN}_x$  is used as a passivation layer. Significant shifts in capacitance, conductance and leakage current characteristics were observed for metal/ $\text{SiN:H}/\text{n}^+\text{-Si}$  MOS capacitor when it was subjected to a constant voltage stress (CVS) of +10V at room temperature. The interface trap density ( $D_{it}$ ) across the  $\text{SiN:H}/\text{n}^+\text{-Si}$  interface increased from  $6.3 \times 10^9$  to  $7.5 \times 10^9 \text{ cm}^{-2}\text{eV}^{-1}$  after a 500-second stress whereas the  $\text{n}^+/\text{p}$  junction diode remained unaffected by the stress. A direct correlation between the degradation of  $\text{SiN:H}/\text{Si}$  interface and the solar cell performance was observed. It is seen that there is a decrease in the open-circuit voltage ( $V_{oc}$ ) from 570 to 550 mV due to CVS. No significant change in short-circuit current ( $I_{sc}$ ) is observed whereas the conversion efficiency ( $\eta$ ) decreases from 12.1 to 11.6% due to CVS. Therefore, the decrease in conversion efficiency by  $\sim 4.13\%$  is due to increase in  $D_{it}$  after 500s stressing. CVS study on  $\text{Cu}/\text{SiN}_x/\text{n}^+$  MOS capacitor both under dark and light illumination is carried out. It is observed that the degradation in solar cell parameters is more when the MOS capacitor is stressed under illumination compared to dark condition. It is also seen that there is a shift in both C-V and G-V characteristics after 5 hrs of light soaking. Thus, an increment in interface trap density ( $D_{it}$ ) is observed after light soaking. Therefore, degradation in solar cell parameters occurs after light soaking due to increase in  $D_{it}$ .

**INFLUENCE OF SiN<sub>x</sub>/Si INTERFACE STATES ON Si SOLAR CELLS**

**by  
Santosh Sahoo**

**A Dissertation  
Submitted to the Faculty of  
New Jersey Institute of Technology  
in Partial Fulfillment of the Requirements for the Degree of  
Doctor of Philosophy in Materials Science and Engineering**

**May 2013**

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## **APPROVAL PAGE**

### **INFLUENCE OF $\text{SiN}_x/\text{Si}$ INTERFACE STATES ON Si SOLAR CELLS**

**Santosh Sahoo**

---

Dr. Nuggehalli M. Ravindra, Dissertation Co-Advisor Professor, Department of Physics, NJIT	Date
---	------

---

Dr. Bhushan Sopori, Dissertation Co-Advisor Principal Engineer, National Renewable Energy Laboratory, Golden, Colorado	Date
---	------

---

Dr. Anthony Fiory, Committee Member Research Professor, Department of Physics, NJIT	Date
--	------

---

Dr. Tao Zhou, Committee Member Associate Professor, Department of Physics, NJIT	Date
--	------

---

Dr. Ken Ahn, Committee Member Assistant Professor, Department of Physics, NJIT	Date
---	------

## BIOGRAPHICAL SKETCH

**Author:** Santosh Sahoo  
**Degree:** Doctor of Philosophy  
**Date:** May 2013

### Undergraduate and Graduate Education:

- Doctor of Philosophy in Materials Science and Engineering  
New Jersey Institute of Technology, Newark, NJ, 2013
- Master of Science in Physics  
Utkal University, Bhubaneswar, Odisha, India
- Bachelor of Science in Physics  
Utkal University, Bhubaneswar, Odisha, India

**Major:** Materials Science and Engineering

### Presentations and Publications:

- S. K. Sahoo, B. L. Sopori, D. Misra, R. Rivero, and N. M. Ravindra, "Impact of interface trap density at the metal/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor in multilayered Si solar cells" submitted to *Applied Physics Letters* March, 2013.
- Bhushan Sopori, S. K. Sahoo, V. Mehta, D. Guhabiswas, and H. Moutinho, "A method for high-quality cross-sectioning of Si solar cells" *IEEE Proceedings*. 978, 001674 (2011).
- Bhushan Sopori, S. K. Sahoo, V. Mehta, D. Guhabiswas, and H. Moutinho, "A method for high-quality cross-sectioning of Si solar cells" presented at 37<sup>th</sup> IEEE special photovoltaic meeting held in Seattle, WA, during 21<sup>st</sup> -25<sup>th</sup> June, 2011.
- Bhushan Sopori, S. K. Sahoo, V. Mehta, D. Guhabiswas, and H. Moutinho, "A cross-section method for Si solar cell" presented at Materials Research Society (MRS) workshop held in Denver, Colorado, during 4-7 October, 2011.
- S. K. Sahoo and D. Misra, "Field dependent electrical conduction in HfO<sub>2</sub>/SiO<sub>2</sub> gate stack for before and after constant voltage stressing" *J. Appl. Phys.* 110, 084104 (2011).
- S. K. Sahoo and D. Misra, "Interfacial layer growth condition dependent carrier transport mechanisms in HfO<sub>2</sub>/SiO<sub>2</sub> gate stacks" *Appl. Phys. Lett.* 100, 232903 (2012).



Dedicated to my father, mother, wife, and son  
With love and gratitude

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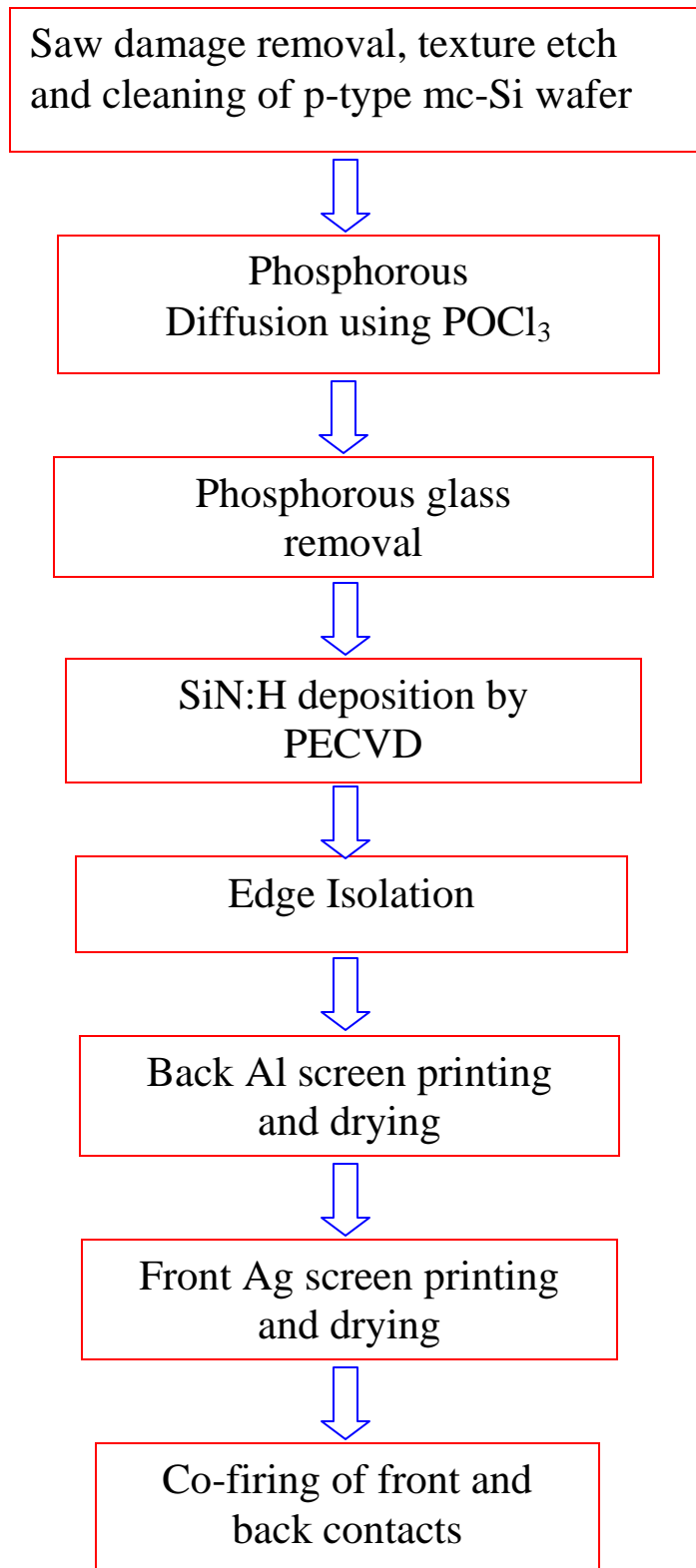
## CHAPTER 1

### INTRODUCTION

#### 1.1 Multicrystalline Si solar cell fabrication

A typical cell fabrication process for screen printed mc-Si is shown in Figure 1.1. P-type mc-Si is cast as ingots using the crystal growth furnace. Wire sawing is used to cut the ingots into wafers of desired thickness (i.e., 160-180  $\mu\text{m}$ ). Next, chemical etching step serves to remove saw damage (10  $\mu\text{m}$ ) and, subsequently, texture etch (i.e., 4-5  $\mu\text{m}$  texture height) the wafers. The wafers are anisotropically etched in alkaline (NaOH + Isopropyl alcohol) or isotropically etched acidic solution (HF + HNO<sub>3</sub> + Water). Wafers are then rinsed and dried.

Next, phosphorus diffusion step is performed on wafer by using either POCl<sub>3</sub>, or dilute H<sub>3</sub>PO<sub>4</sub> to form n<sup>+</sup> type layer on p type wafer. It is a high temperature step carried out at 900°C for 25 minutes. The phosphor glass is then removed by acid etching. Sheet resistance of n<sup>+</sup> layer (also called as emitter) is usually maintained at 40-50  $\Omega/\square$ . A non stoichiometric SiN:H based anti-reflection coating (70-80 nm thick with refractive index of  $\sim 2.0$ ) is deposited using PECVD technique. The cell is edge isolated using plasma etch. Gridded Ag based front (25 micron in thickness) and back (whole area) Al based paste (7-10 mg/cm<sup>2</sup>) are screen printed to serve as contacts. Cells are fired using fire-through contact metallization technique.



**Figure 1.1** mc-Si solar cell processing flow chart.

## 1.2 Optical Processing Furnace

The screen printed mc-Si solar cells are fired in optical processing furnace (OPF) which is developed by Dr. Bushan Sopori at National Renewable Energy Laboratory (NREL). In the OPF, the process is controlled by the optical power delivered to the device. This process uses spectrally selected light to create a controlled uniform local melt at an illuminated semiconductor-metal interface. This melt forms an alloyed region that regrows epitaxially on the silicon substrate to form highly reflective, Ohmic contact of extremely low contact resistivity ( $< 10^{-4} \Omega\text{-cm}^2$ ).<sup>1</sup> OPF is used to make both front and back contacts.

## 1.3 Thesis Outline

In Chapter 1, the process flow for the fabrication of mC-Si solar cell is presented. The usefulness of optical processing furnace for making front and back contact is given. The effect of light soaking, constant voltage stress (CVS), both in dark and light illumination conditions, on the photovoltaic parameters are discussed.

In Chapter 2, the theory of the current-voltage (I-V) characteristics, under dark and illumination conditions, is given. Basic equations for solar cell parameters are presented. The capacitance-voltage (C-V) characteristics of the p-n junction are presented. The C-V characteristics of MOS capacitor and the estimation of interface trap density ( $D_{it}$ ) by various methods are presented. The calculation of fixed charge density ( $Q_f$ ) in the dielectric is also summarized.

In Chapter 3, the various equipment that are used for electrical measurements are discussed. Keithley 238 high current source measure unit is used for taking transient

current [current-time (I-t)] and I-V measurements and HP 4284A precision LCR meter is used for making C-V and conductance-voltage (G-V) measurements.

In Chapter 4, the effect of light soaking on both C-V and G-V characteristics is discussed. Both optical and thermal effects as well as only optical effect on C-V and G-V plots are also presented.

In Chapter 5, the effect of constant voltage stress (CVS) on Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor and its impact on the Si solar cell parameters are presented. The correlation between the degradation of solar cell parameters and the interface trap density (D<sub>it</sub>) at SiN<sub>x</sub>/n<sup>+</sup>Si is summarized.

In Chapter 6, the constant voltage stress (CVS) study on Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor, both in dark and illumination conditions, is presented. The impact of interface trap density (D<sub>it</sub>) on solar cell parameters for CVS under dark and light conditions are given.

Chapter 7 focuses on the conclusions based on studies performed in Chapters 1-6.

## **1.4 Light Soaking**

When Si solar cell is kept under light for several hours, interface traps are created at the SiN<sub>x</sub>/n<sup>+</sup> interface. These traps are responsible for the surface recombination. As a result, there is loss of generated carriers by illumination due to these interface traps. Thus, degradation occurs in Si solar cell performance. The quality of SiN<sub>x</sub> passivation layer plays a vital role in this degradation process.

### **1.5 Constant Voltage Stress (CVS)**

By the application of a constant positive bias to the gate terminal of a MOS capacitor for some time interval, there will be flow of electrons from the semiconductor towards the gate. As a result, these electrons will create Si dangling bonds at the dielectric/semiconductor interface. These Si dangling bonds are interface traps ( $D_{it}$ ). The interface traps participate in surface recombination mechanisms. Hence, the solar cell parameters will be degraded by this constant voltage stress on the  $\text{Cu/SiN}_x/\text{n}^+$  MOS capacitor.

### **1.6 Constant Voltage Illumination Stress (CVIS)**

In constant voltage illumination stress, a constant positive bias is applied to the gate terminal of the MOS capacitor under light illumination. Electron-hole pairs are created in the semiconductor under illumination. Due to the application of positive bias on the gate terminal, these generated electrons, by the incident light, will move towards the gate. These electrons will create Si dangling bonds resulting in interface traps ( $D_{it}$ ) at the dielectric/Si interface and also some of the electrons will be trapped by the bulk traps in the dielectric. In Si solar cells, interface traps will be created at the  $\text{SiN}_x/\text{n}^+$  interface as well as some light generated electron carriers will be trapped by the bulk defects in the  $\text{SiN}_x$ . Thus, the Si solar cell parameters will be degraded more by this constant voltage stress under illumination compared to CVS carried out in dark condition.

## CHAPTER 2

### THEORY

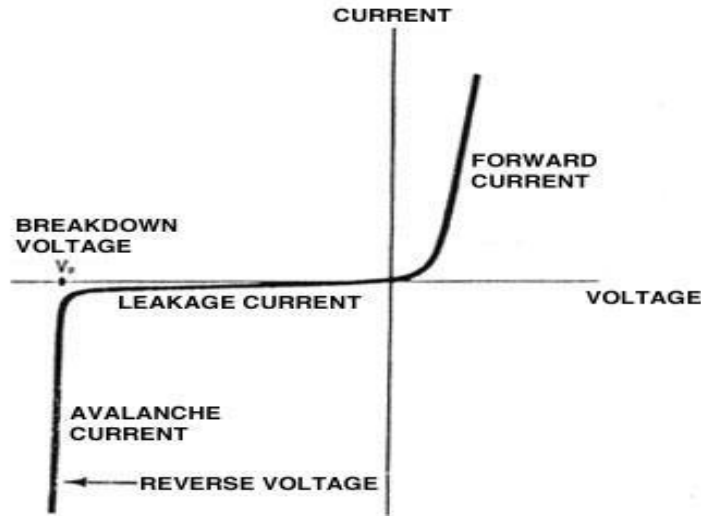
#### 2.1 I-V characteristics of p-n junction

The total current in a p-n junction is given by,

$$J = J_s (e^{qV/kT} - 1) \quad (2.1)$$

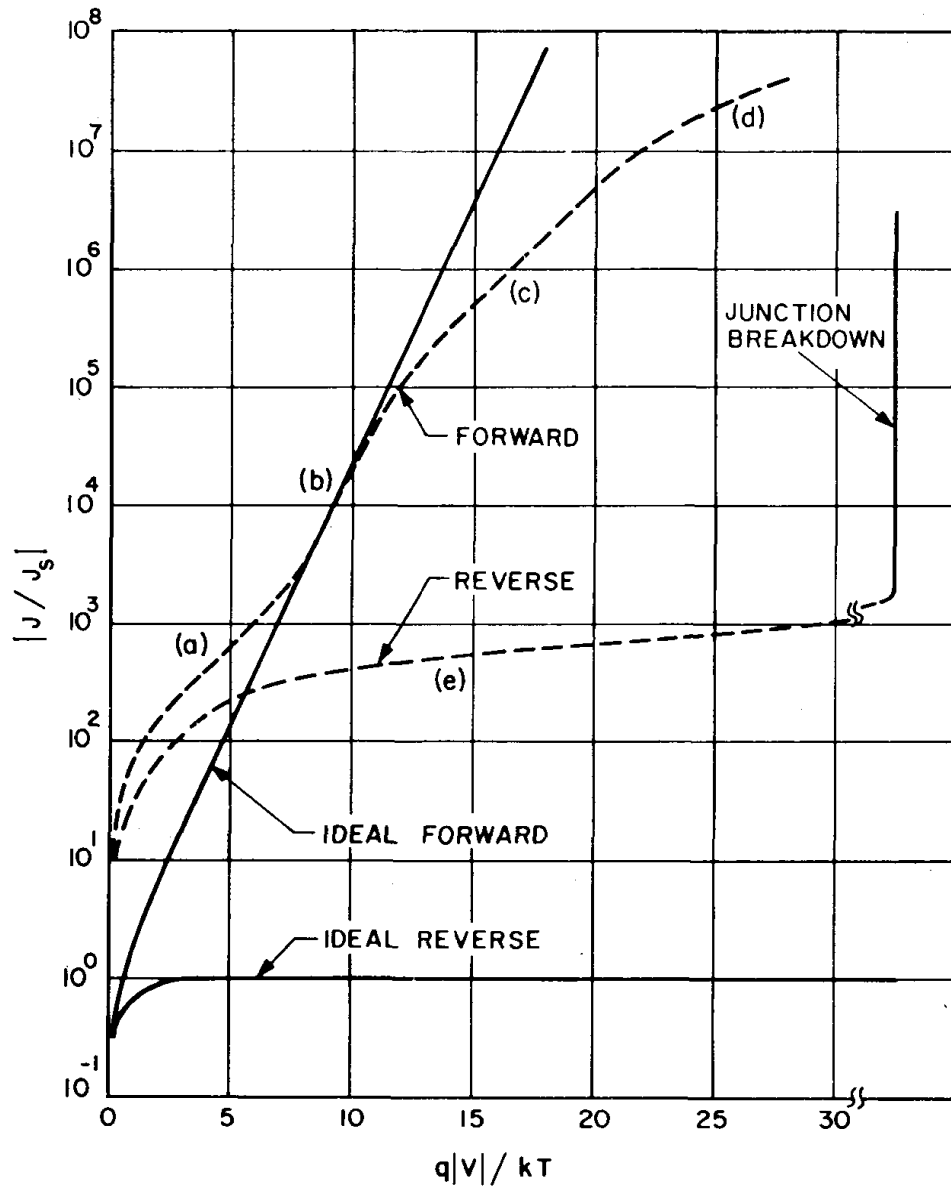
$$\text{where, } J_s = \frac{qD_p p_n}{L_p} + \frac{qD_n n_p}{L_n} \quad (2.2)$$

Here  $J_s$  is the saturation current and Equation (2.2) is the Shockley equation.  $D_p$  and  $D_n$  are the diffusion co-efficients, whereas  $L_p$  and  $L_n$  are the diffusion lengths for electron and hole, respectively. Figure 2.1 shows the ideal current-voltage characteristics of a p-n junction diode. For Si p-n junctions, the ideal equation can give only qualitative agreement with measurements.



**Figure 2.1** Ideal current-voltage characteristics.

In the case of a practical Si p-n junction diode, the departure from the ideal are mainly due to the following: (1) surface effects, (2) generation and recombination of carriers in the depletion layer, (3) tunneling of carriers between states in the bandgap, (4) high-injection condition that may occur even at relatively small forward bias, and (5) series resistance effects. Figure 2.2 shows the I-V characteristics of a practical Si junction diode in a semilog plot.



**Figure 2.2** Current-voltage characteristics of a practical Si diode.<sup>2</sup>

It is observed that the current is contributed by various mechanisms in different voltage regions. In the low voltage region, the current is due to generation-recombination current. For the medium voltage region, the current is due to diffusion and high injection effect whereas the high voltage region current is because of the series resistance effects. The current in the reverse bias condition is due to generation current which is due to the generation in the depletion region. This generation current is given by,<sup>2</sup>

$$J_{gen} = \int_0^W qUdx = qUW = \frac{qn_i W}{\tau_e} \quad (2.3)$$

where, W is the depletion-layer width, U is the recombination rate,  $n_i$  is the intrinsic carrier concentration, and  $\tau_e$  is the minority carrier life time.

At forward bias, the major recombination-generation processes, in the depletion region, are the capture processes. The total current is due to a recombination current  $J_{rec}$  and the diffusion current. The recombination current is given by,<sup>2</sup>

$$J_{rec} = \int_0^W qUdx \approx \frac{qW}{2} \sigma v_{th} N_t n_i \exp\left(\frac{qV}{2kT}\right) \quad (2.4)$$

where,  $N_t$  is the trap density,  $\sigma$  is the capture cross-section, and  $v_{th}$  is the thermal velocity.

The total forward current is the sum of diffusion and recombination current and is given by,<sup>2</sup>

$$J_F = q \sqrt{\frac{D_p}{\tau_p}} \frac{n_i^2}{N_D} \exp\left(\frac{qV}{kT}\right) + \frac{qW}{2} \sigma v_{th} N_t n_i \exp\left(\frac{qV}{2kT}\right) \quad (2.5)$$

where, q is the electronic charge,  $\tau_p$  is the minority carrier lifetime for holes, and  $N_D$  is the concentration for donors.

The experimental results, in general, can be represented by the semi-empirical form,<sup>2</sup>

$$J_F \sim \exp\left(\frac{qV}{nkT}\right) \quad (2.6)$$

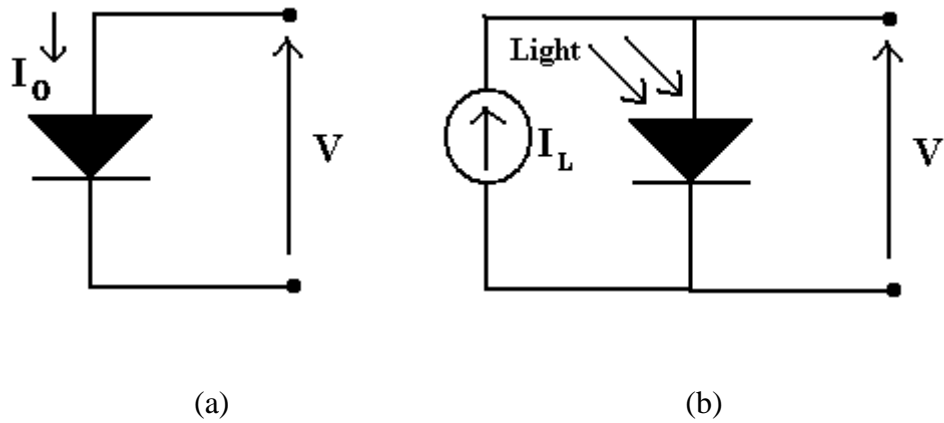


where, the factor  $n$  equals to 2 when the recombination current dominates and  $n$  equals to 1 when the diffusion current dominates the current conduction mechanism. When both currents are comparable,  $n$  has value between 1 and 2.

For the high injection condition, the current is roughly proportional to  $\exp(qV/2kT)$  with  $n$  equal to 2. At high injection level, there is another effect associated with the finite resistivity in the quasi-neutral regions of the junction. This resistance accounts for an appreciable amount of the voltage drop between the diode terminals. This effect is called the series resistance effect.

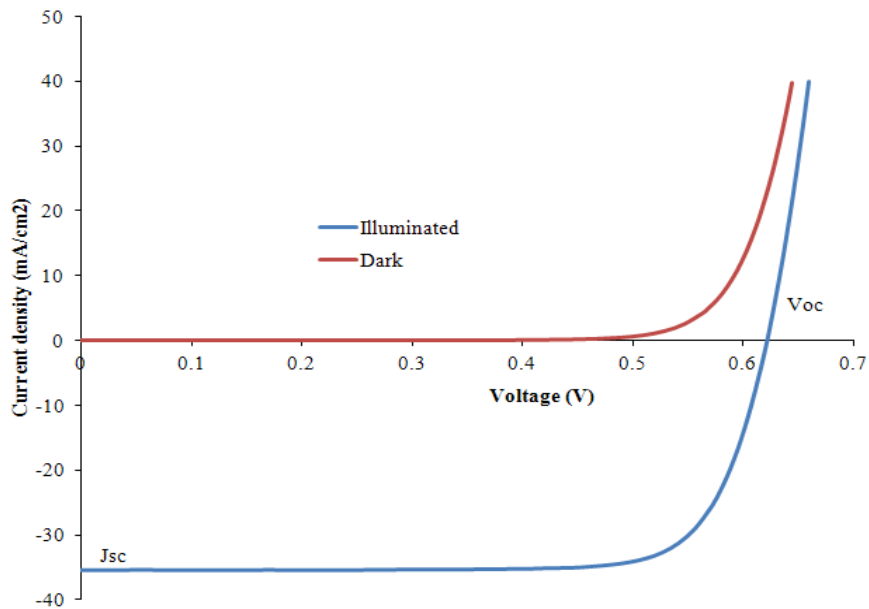
## **2.2 I-V Characteristics of p-n Junction Diode under Illumination**

A solar cell is simply a p-n junction diode as shown in Figure 2.3 (a). It consists of a potential barrier at the junction which creates an electric field. When light shines on a solar cell (Figure 2.3 (b)), the photons with energy greater than the band gap create electron-hole pairs.<sup>3</sup> The dark I-V characteristics of a junction diode are well known and are shown in Figure 2.4. Because of the electric field present at the junction, the electrons in the p-region move towards the n-side of the junction and the holes in the n-region move towards the p-side of the junction. The result is an extra component of current flowing in the opposite direction. This is called light induced current ( $I_L$ ) or short circuit current ( $I_{sc}$ ). Because  $I_L$  flows in the opposite direction under light, the light I-V characteristics of the solar cell shifts downwards as shown in Figure 2.4.



**Figure 2.3** (a) P-N junction diode (solar cell) and (b) P-N junction diode (solar cell) under light illumination.

The basic steps in the operation of solar cells are the generation of light generated carriers, the collection of these carriers to generate current, and the generation of a large voltage across the solar cell, as well as the dissipation of power in the load and in parasitic resistances.<sup>4</sup>



**Figure 2.4** I-V characteristics of a solar cell under dark and light illumination conditions.

The important parameters of solar cells are  $I_{sc}$  (short-circuit current),  $V_{oc}$  (open-circuit voltage), FF (fill factor), and  $\eta$  (conversion efficiency). The  $I_{sc}$  is the current through the solar cell when the voltage across the solar cell is zero. The short-circuit current is due to the generation and then separation of light generated carriers. The  $V_{oc}$  is the maximum voltage available from the solar cell. This occurs at zero current. The  $V_{oc}$  corresponds to the amount of forward bias on the solar cell due to the bias of the solar cell junction with the light-generated current. FF determines the maximum power from a solar cell. The FF is defined as the ratio of the maximum power from the solar cell to the product of  $I_{sc}$  and  $V_{oc}$ . The  $\eta$  is the important parameter to compare the performance of one solar cell to another.  $\eta$  is defined as the ratio of energy output from the solar cell to the input energy from the sun.<sup>4</sup>

The expression for the solar cell parameters are given by the following equations:

$$I_L = qAG (L_n + W + L_p) \quad (2.7)$$

$$V_{oc} = \frac{kT}{q} \ln \left( \frac{I_L}{I_s} + 1 \right) \quad (2.8)$$

$$FF = \frac{I_m V_m}{I_{sc} V_{oc}} \quad (2.9)$$

$$\eta = \frac{I_m V_m}{P_{in}} = \frac{I_{sc} V_{oc} FF}{P_{in}} \quad (2.10)$$

where, A is the area of the cell, W is the depletion layer width,  $L_p$  and  $L_n$  are the diffusion lengths for electrons and holes,  $I_L$  is the current due to illumination,  $I_s$  is the saturation current,  $I_m$  and  $V_m$  are the maximum current and voltage, respectively corresponding to the maximum power.

The p-n junction solar cell can be expressed by either single diode model (as shown in Figure 2.5) or two diode model (as shown in Figure 2.6). The equivalent circuit for one diode model is shown in Figure 2.5, where a constant-current source is in parallel with the junction. The source  $I_L$  results from the excitation of excess carriers by solar radiation;  $I_s$  is the diode saturation current, and  $R_L$  is the load resistance. The I-V characteristics of such a device are given by,

$$I = I_s (e^{qV/kT} - 1) - I_L \quad (2.11)$$

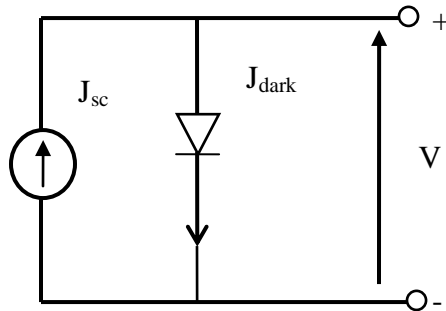
In the analysis of solar cells and to calculate their performance parameters, some research groups analyzed solar cell by the single exponential diode model. Some other groups analyzed solar cells by the two diode model.

Most of the people analyzed solar cells by single diode model to determine the ideality factor and series resistance. It is difficult to analyze the properties of a solar cell by the single equivalent diode model. The equivalent circuit for a two-diode model is given in Figure 2.6. The diode current for a two diode model is given by Equation (2.12),

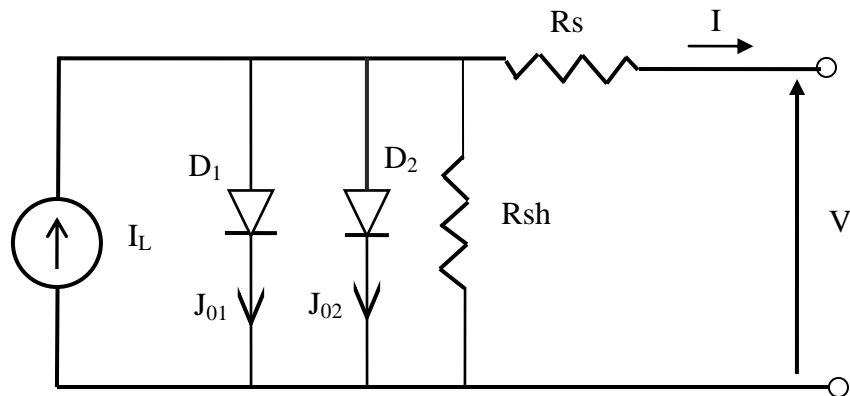
$$I = I_{01} \left\{ \exp \left( \frac{q(V - IR_s)}{kT} \right) - 1 \right\} + I_{02} \left\{ \exp \left( \frac{q(V - IR_s)}{2kT} \right) - 1 \right\} + \left( \frac{V - IR_s}{R_{sh}} \right) - I_L \quad (2.12)$$

where,  $I_{01}$  and  $I_{02}$  are the saturation currents,  $k$  is the Boltzman's constant,  $T$  is the temperature,  $q$  is the electronic charge,  $R_s$  is the series resistance, and  $R_{sh}$  is the shunt resistance. The first term in Equation (2.12) is due to the recombination current in the quasi neutral region (from the first diode) and the second term is due to the recombination current in the depletion region (from the second diode). The correct values

of these parameters are very important to find in large area solar cells because these parameters provide information about various losses.



**Figure 2.5** Equivalent circuit of a solar cell showing one diode model.



**Figure 2.6** Two diode model of a solar cell.

### 2.3 C-V Characteristics of p-n Junctions

There are basically two types of capacitance associated with a junction: (1) the junction capacitance or depletion layer capacitance due to the dipole in the transition region and (2) the charge storage capacitance or the diffusion capacitance arising from the lagging behind of voltage as current changes, due to charge storage effects. Both of these capacitances are important, and they must be considered in designing p-n junction devices for use with time-varying signals. The depletion layer capacitance (1) is dominant under reverse-bias conditions, and the diffusion capacitance (2) is dominant when the junction is forward biased.

The depletion layer capacitance is given by,<sup>5</sup>

$$C_j = \frac{dQ}{dV} \quad (2.13)$$

$$C_j = \frac{dQ}{d(V_0 - V)} = \frac{A}{2} \left[ \frac{2q\epsilon}{(V_0 - V)} \frac{N_d N_a}{N_d + N_a} \right]^{1/2} \quad (2.14)$$

where, A is the area of the junction,  $N_d$  and  $N_a$  are the concentration of donors and acceptors respectively, and  $\epsilon$  is the permittivity of the semiconductor.

$$C_j = \epsilon A \left[ \frac{q}{2\epsilon(V_0 - V)} \frac{N_d N_a}{N_d + N_a} \right]^{1/2} = \frac{\epsilon A}{W} \quad (2.15)$$

where, W is the depletion layer width and is given by,

$$W = \left[ \frac{2\epsilon(V_0 - V)}{q} \left( \frac{N_a + N_d}{N_a N_d} \right) \right]^{1/2} \quad (2.16)$$

In analogy with the parallel plate capacitor, the depletion layer width W corresponds to the plate separation of the conventional capacitor.

In the case of an asymmetrically doped junction, the transition region extends primarily into the less heavily doped side, and the capacitance is determined by only one of the doping concentrations. For  $n^+$ -p junction (Si solar cell),  $N_d \gg N_a$ . The capacitance is then given by,<sup>5</sup>

$$C_j = \frac{A}{2} \left[ \frac{2q\epsilon}{V_0 - V} N_a \right]^{1/2} \quad \text{for } n^+ \text{-p junction} \quad (2.17)$$

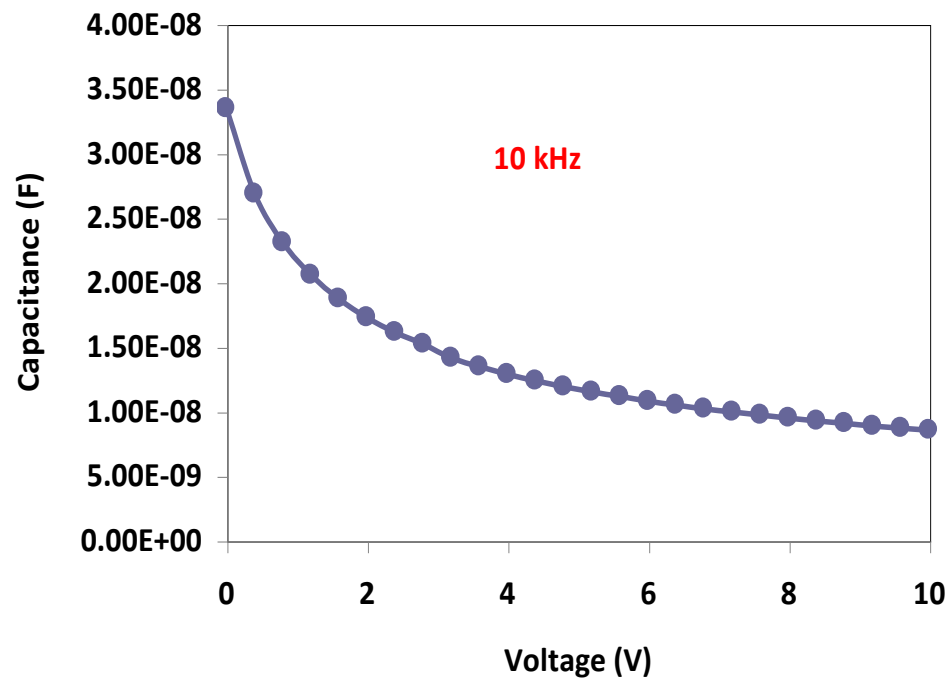
It is, therefore, possible to obtain the doping concentration of the lightly doped p region (base region of Si solar cell) from a measurement of capacitance.

$$\frac{1}{C^2} = \frac{1}{A^2} \frac{2(V_0 - V)}{q\epsilon N_a} \quad (2.18)$$

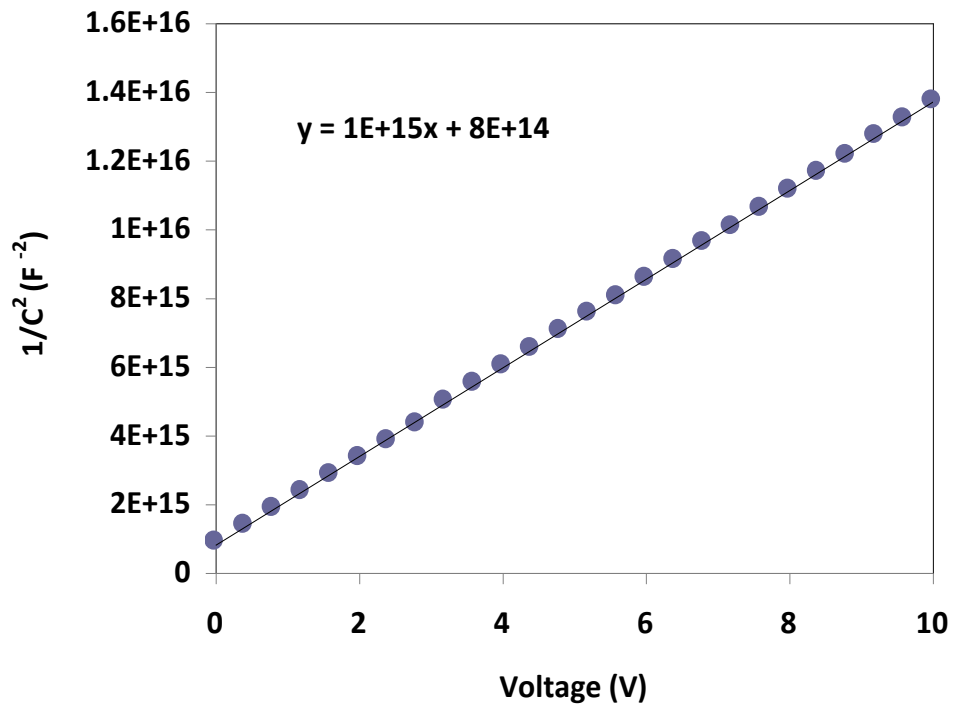
$$\frac{d(1/C^2)}{dV} = \frac{1}{A^2} \frac{2}{q\epsilon N_a} \quad (2.19)$$

It is clear from Equation (2.19) that, by plotting  $1/C^2$  versus  $V$ , a straight line should result for a one-sided abrupt junction. The slope gives the doping concentration of the substrate ( $N_a$ ), and the intercept gives the built in potential ( $V_{bi}$ ).

Figure 2.7 shows the capacitance versus voltage (C-V) for the reverse bias condition for a  $n^+$ -p junction Si solar cell. The depletion layer capacitance decreases as the reverse bias voltage increases due to the increase in the width of the transition region. Figure 2.8 shows the  $1/C^2$  versus voltage ( $1/C^2 - V$ ) plot for the same data points shown in Figure 2.7. It is observed that the plot is a straight line and its slope will give the doping concentration ( $N_a$ ) of the base region (p region in Si solar cell).



**Figure 2.7** Capacitance vs. voltage (C-V) characteristic of a Si solar cell at 10 kHz.

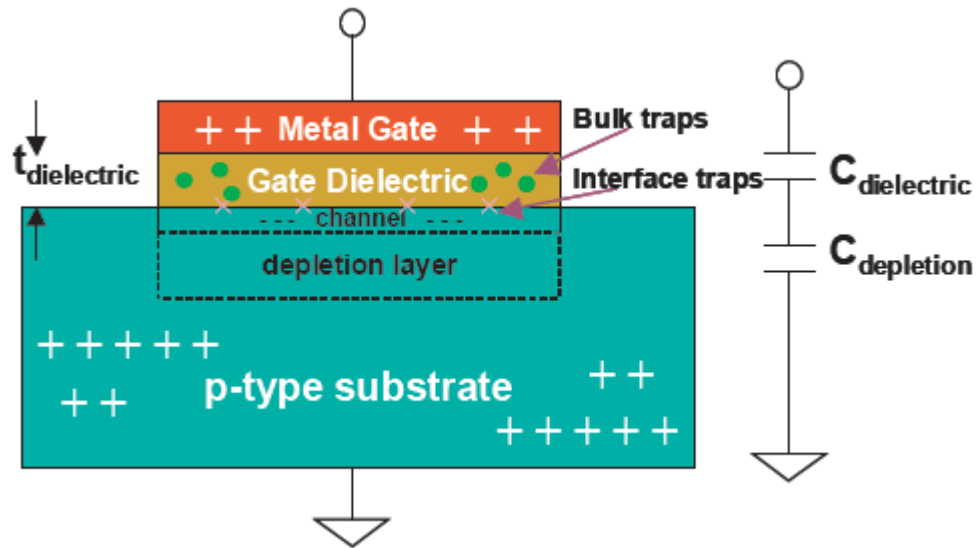


**Figure 2.8**  $1/C^2$  vs. V plot of a Si solar cell at 10 kHz.



## 2.4 C-V Characteristics of MOS Capacitor

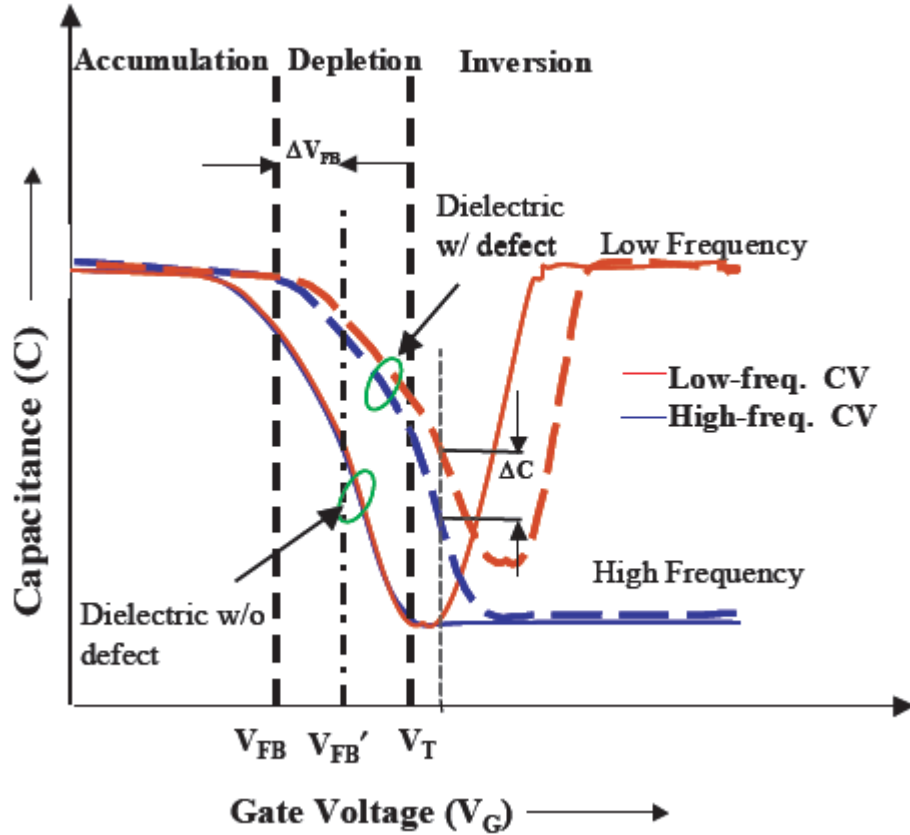
When a voltage is swept across the MIS device, the semiconductor surface goes through an accumulation of majority carriers, depletion of majority carriers, or inversion with minority carriers. As an example, consider a p-type semiconductor for the MIS device and apply a negative potential to the metal electrode (gate); the mobile positive holes, the majority carriers, accumulate at the dielectric-semiconductor interface during accumulation. These carriers form a thin layer, which acts much like a parallel plate capacitor equal in area to the gate. Once the voltage is raised to a small positive value, the holes are repelled, causing depletion. Raising the voltage further attracts electrons to the interface. The electrical equivalent circuit of a MIS capacitor is, therefore, a series combination of a fixed voltage-independent gate oxide (insulator) capacitance and a voltage-dependent semiconductor capacitance due to depletion as shown in Figure 2.9.



**Figure 2.9** A metal/insulator/semiconductor (p-type) (MIS) structure is shown that is used extensively to characterize dielectric films. Dielectric/semiconductor interface traps and bulk traps are shown. For positive gate bias, semiconductor and metal gate act as cathode and anode, respectively, whereas, for negative gate bias, the opposite holds. The equivalent circuit of the series capacitance of dielectric and depletion capacitances is also provided.<sup>6</sup>

Figure 2.10 shows the C-V characteristics of MIS structures with a dielectric deposited on a p-type semiconductor. Both the cases of dielectric with and without traps (ideal case) are considered. The capacitance in the accumulation region is defined by the gate area ( $A$ ) and the dielectric thickness ( $t_{\text{dielectric}}$ ) and is designated as  $C_{\text{dielectric}}$  (accumulation capacitance). The dielectric constant ( $k$ ) can be obtained from the following equation,

$$K = \frac{C_{\text{dielectric}} t_{\text{dielectric}}}{A} \quad (2.20)$$



**Figure 2.10** High-frequency (hf) and low-frequency (lf) C-V characteristics of MIS structure for dielectric films with and without (ideal) defects are shown. Flatband voltage shift of hf C-V,  $\Delta V_{\text{FB}} = (V_{\text{FB}}' - V_{\text{FB}}) > 0$  indicates negative charge trapping. For a film with defects, stretch-out of hf C-V, and offset in capacitance,  $\Delta C$ , in between hf and lf C-V indicate the presence of interface traps.<sup>6</sup>

Interface traps cause an offset in between low-frequency and high-frequency C-V plots ( $\Delta C$ ) as shown in Figure 2.10. This offset can be utilized to calculate the interface trap density ( $D_{it}$ ) from the measured high-frequency capacitance ( $C_{hf}$ ) and low-frequency capacitance ( $C_{lf}$ ) at a certain gate bias as below.<sup>6</sup>

$$D_{it} = \frac{C_{dielectric}}{q} \left( \frac{C_{lf} / C_{dielectric}}{1 - C_{lf} / C_{dielectric}} - \frac{C_{hf} / C_{dielectric}}{1 - C_{hf} / C_{dielectric}} \right) \quad (2.21)$$

Here,  $q$  is the charge of an electron.  $D_{it}$  can be measured for different gate biases in the depletion regime.

Larger inaccuracies arise in extracting  $D_{it}$  by the above low and high frequency method because the difference between two capacitances must be used. In the conductance method, this problem does not occur as the measured conductance is directly related to the interface traps.

Energy loss, which is due to capture/emission of carriers by interface traps, is represented by an equivalent conductance,  $G_p$ , of the MIS structure.  $G_p$ , measured over a wide range of frequencies and gate voltages, is a measure of  $D_{it}$  with respect to gate bias.

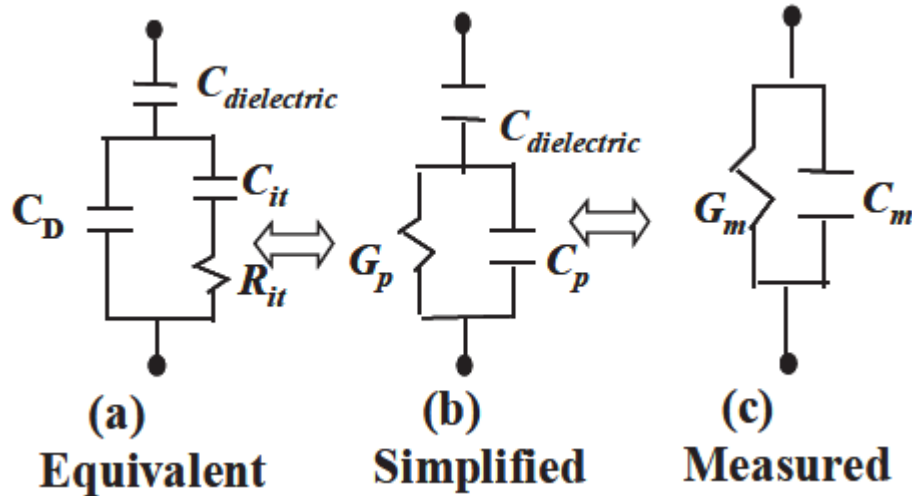
An equivalent circuit, as shown in Figure 2.11 (a), represents an MIS structure with interface traps. Here,  $R_{it}$  represents the energy loss due to interface traps, while  $C_{it}$  represents the capacitance due to charge stored in these traps. Formation of a depletion region, whose capacitance is represented by  $C_D$ , takes place along with interaction of semiconductor carriers with interface traps. Hence,  $C_D$  is shown in parallel with the series combination of  $C_{it}$  and  $R_{it}$ . Storage of charge across the dielectric material occurs in addition to that in the depletion region and at the interface traps. Thus,  $C_{dielectric}$  remains in series with the network mentioned above. A simplified circuit (Figure 2.11(b)) contains

the parallel combination of equivalent conductance,  $G_p$ , and capacitance  $C_p$ , which can be derived from the parallel network of Figure 2.11 (a). The measured conductance,  $G_m$ , and capacitance,  $C_m$ , are also indicated (Figure 2.11 (c)) across the two-terminal MIS structure using conventional measurement instruments (e.g., HP 4284A LCR meter). To find  $G_p$  from the measured data, the following Equation is used<sup>6</sup>

$$G_p = \frac{\omega^2 G_m C_{dielectric}^2}{G_m^2 + \omega^2 (C_{dielectric} - C_m)^2} \quad (2.22)$$

where,  $\omega = 2\pi f$  is the radian frequency.  $G_p$  is estimated as a function of both gate bias and frequency, especially in the depletion regime.  $D_{it}$  can be calculated from the highest value of  $G_p/\omega$  using the following equation.<sup>6</sup>

$$D_{it} = \frac{2.5}{q} \left( \frac{G_p}{\omega} \right)_{\max} \text{ cm}^{-2} \text{ eV}^{-1} \quad (2.23)$$



**Figure 2.11** (a) Equivalent circuit of MIS structures with interface traps.  $R_{it}$  and  $C_{it}$  represent interface traps induced energy loss and charge storage respectively. (b) Simplified circuit, derived from (a), for analysis. Equivalent conductance  $G_p$ , is computed from measured data as a function of both test (ac) signal frequency and gate bias (dc). (c) Circuit representing parallel capacitance ( $C_m$ ) and conductance ( $G_m$ ), which are measured across two-terminal MIS structures for different frequencies and biases using conventional instruments (e.g., HP 4284A precision LCR meter).<sup>6</sup>

### The fixed charge density ( $Q_f$ )

For an ideal MOS capacitor (no fixed charges in the dielectric), the flat band voltage is given by,<sup>2</sup>

$$V_{FB} = \Phi_{ms} \quad (2.24)$$

where,  $\Phi_{ms} = \Phi_m - \Phi_s$  is the difference between the work function of metal and that of the semiconductor.

If a fixed surface charge density  $Q_f$  exists at the semiconductor-insulator interface, the experimental capacitance-voltage curve will be displaced from the ideal theoretical curve by an amount,<sup>2</sup>

$$V_{FB} = \Phi_{ms} - \frac{Q_f}{C_i} \quad (2.25)$$

where,  $V_{FB}$  is the shift in voltage corresponding to the flat-band capacitance, and  $C_i$  is the insulator capacitance. The fixed oxide charge density can be obtained from Equation (2.25) by,<sup>2</sup>

$$Q_f = C_i (\Phi_{ms} - V_{FB}) \text{ coulomb/cm}^2 \quad (2.26)$$

$$Q_f = \frac{C_i}{q} (\Phi_{ms} - V_{FB}) \text{ charges/cm}^2 \quad (2.27)$$

## CHAPTER 3

### EXPERIMENTAL

#### 3.1 Experimental Techniques and Analysis

To experimentally determine the effect of light illumination and constant voltage stressing (CVS), we have used multicrystalline Si (mc-Si) solar cells of smaller dimensions. The cells were fabricated on high quality (the resistivity is of  $\sim 2 \Omega\cdot\text{cm}$  and the minority carrier life time is about  $100 \mu\text{s}$ ) wafers. The doping of  $n^+$  emitter layer is  $10^{18} \text{ cm}^{-3}$ . The passivation  $\text{SiN}_x$  layer which also acts as an anti reflection coating (ARC) was deposited by plasma enhanced chemical vapor deposition (PECVD) process on the emitter layer and its thickness was  $800 \text{ \AA}$ . The following section discusses the experimental techniques and equipments that are used for the characterization of both  $\text{Cu/SiN}_x/n^+$  MOS capacitor and  $p\text{-}n^+$  junction diodes.

#### 3.2 Diode Prober and Electrical Characterization

The experimental setup consists of a Rucker & Kolls (R&K) Model 680 wafer prober, a Keithley 238 Source Measure Device, and a Hewlett Packard 4248A precision LCR Meter that are connected to a computer via a GPIB (General Purpose Interface Bus) interface. Customized software written in LabVIEW is used to control the three instruments. The R&K Model 680 is a precision x-y table that can move a probe table up and down to make temporary contact with a device. A wafer, with many devices on it, is loaded on to the R&K Model 680 that is programmed to probe each device on the wafer. This model accommodates up to 150 mm diameter wafers. The X-Y stages are motorized. The Z stage has a fixed travel of 0.3 mm and is vacuum controlled. A

micrometer provides adjustable probe tip over travel. A manual theta control, located below the vacuum chuck, offers quick and easy adjustment. The Keithley 238 high current source measure unit is used to measure the current versus voltage (I-V) on a specific device both in dark and illumination conditions. The HP 4248A precision LCR meter is used to measure various device parameters as function of both voltage and frequency, i.e., capacitance versus voltage (C-V), capacitance versus frequency (C-f) conductance versus voltage (G-V), conductance versus frequency (G-f), dissipation factor ( $\tan \delta$ ), admittance, impedance, inductance, and resistance of a device.

Keithley 238 high current source measure unit and the R&K Model 680 diode prober are used to take both the constant voltage stress (CVS) and the leakage current measurements of  $\text{Cu/SiN}_x/\text{n}^+$  MOS capacitor. They are also used to acquire the measurements of both the dark and light I-V of  $\text{p/n}^+$  junction diodes.

In this work, HP 4248A precision LCR meter and the R&K Model 680 diode prober are used to take both the capacitance vs. voltage (C-V) and conductance vs. voltage (G-V) measurements at a fixed frequency and oscillation voltage level for  $\text{Cu/SiN}_x/\text{n}^+$  MOS capacitor as well as  $\text{p/n}^+$  junction diode. From the C-V and G-V curves, the interface trap density ( $D_{it}$ ) at the  $\text{SiN}_x/\text{n}^+$ -Si interface was determined.

### **3.3 Light Induced Degradation**

A multicrystalline Si (mc-Si) solar cell of area  $< 1 \text{ cm}^2$  is used for the study of the effect of light illumination on the density of interface trap states at the  $\text{SiN}_x/\text{n}^+$  interface of a Si solar cell. The Si solar cell sample was kept for light soaking for various interval of time under the lamp on the chuck of the diode prober. Both capacitance versus voltage (C-V) and conductance versus voltage (G-V) measurements are taken for the entire Si solar cell

before light soaking (fresh samples). Without disturbing the copper probe contact, both C-V and G-V are also taken after light soaking. The lamp was switched off after performing the light soaking measurements for the required interval of time. After light soaking, the temperature of the chuck reached 37°C. After the lamp is switched off, the C-V and G-V measurements are made at various time intervals and these measurements are continued until the chuck has reached room temperature.

### **3.4 Constant Voltage Stress (CVS) Induced Degradation**

Multicrystalline Si (mc-Si) solar cells of area  $< 1 \text{ cm}^2$  are used for the study of the effect of constant voltage stressing (CVS) on the  $\text{Cu/SiN}_x/\text{n}^+$  MOS capacitor in a Si solar cell device and its impact on the solar cell performance. The Si solar cell sample was kept on the chuck of the diode prober. A constant voltage stress of +10 V was applied to the gate terminal (Cu) of the MOS capacitor in the Si solar cell for various time intervals. Both C-V and G-V measurements, at 10 kHz, are taken for both  $\text{Cu/SiN}_x/\text{n}^+$  MOS capacitor and  $\text{p-n}^+$  junction diode for fresh as well as stressed devices. Interface trap density ( $D_{it}$ ), at the  $\text{SiN}_x/\text{n}^+$  interface, has been calculated for different stress times due to CVS. After different stress times, the light I-V for  $\text{p-n}^+$  junction diode has been taken. Finally, the degradation in solar cell parameters, such as open-circuit voltage ( $V_{oc}$ ), short-circuit current ( $I_{sc}$ ), and conversion efficiency ( $\eta$ ) with the change in interface trap density ( $D_{it}$ ), due to CVS are correlated.



### 3.5 Constant Voltage Illumination Stress (CVIS) Induced Degradation

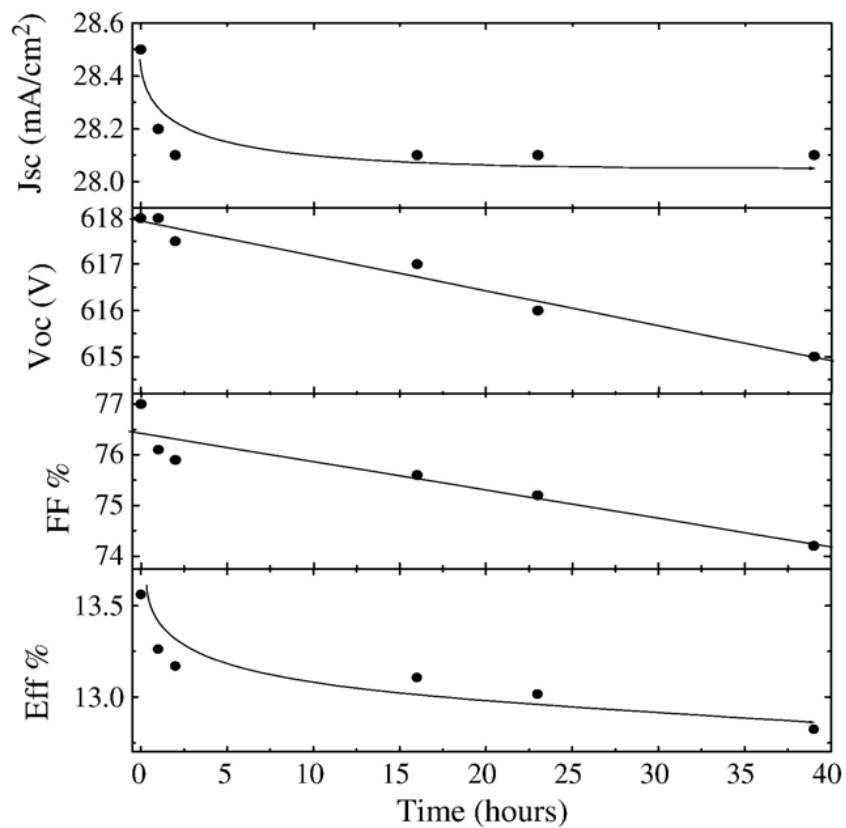
Multicrystalline Si (mc-Si) solar cells of area  $\sim 1.3 \text{ cm}^2$  are used for the study of the effect of constant voltage stressing (CVS) both in dark and light illumination conditions on the  $\text{Cu/SiN}_x/\text{n}^+$  MOS capacitor in a Si solar cell device and its impact on the solar cell parameters. The Si solar cell sample was kept on the chuck of the diode prober. A constant voltage stress of +10 V was applied to the gate electrode (Cu) of the MOS capacitor in the Si solar cell for different interval of times both in dark and illumination conditions. Both C-V and G-V measurements are taken at 10 kHz for both  $\text{Cu/SiN}_x/\text{n}^+$  MOS capacitor and  $\text{p-n}^+$  junction diode for fresh and stressed devices. Interface trap density ( $D_{it}$ ), at the  $\text{SiN}_x/\text{n}^+$  interface, has been calculated for different stress times due to CVS under dark and light conditions. After different stress times, the light I-V for  $\text{p-n}^+$  junction diode has also been taken. Finally, the degradation in solar cell parameters such as open-circuit voltage ( $V_{oc}$ ), short-circuit current ( $I_{sc}$ ), and conversion efficiency ( $\eta$ ), with the change in interface trap density ( $D_{it}$ ), due to CVS in illumination and dark conditions are correlated.

## CHAPTER 4

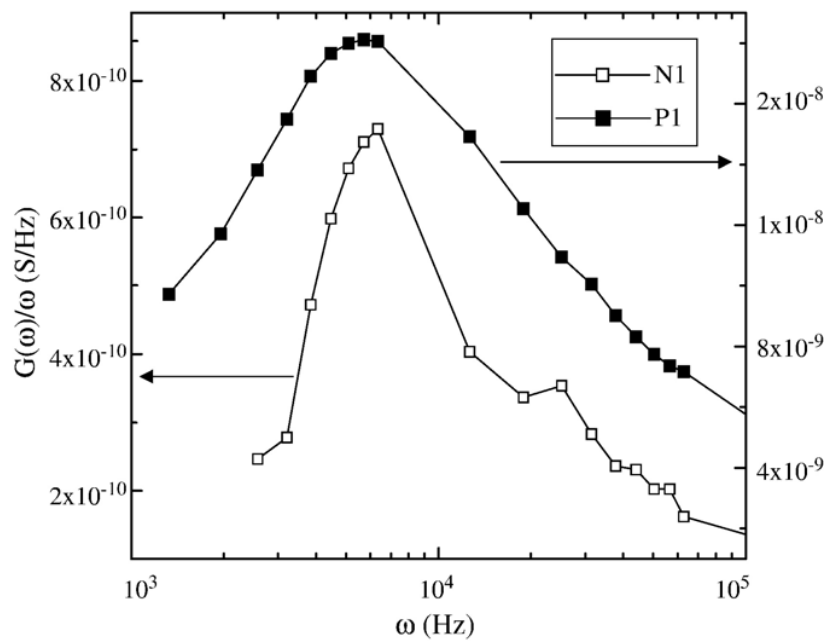
### LIGHT INDUCED DEGRADATION

#### 4.1 Introduction

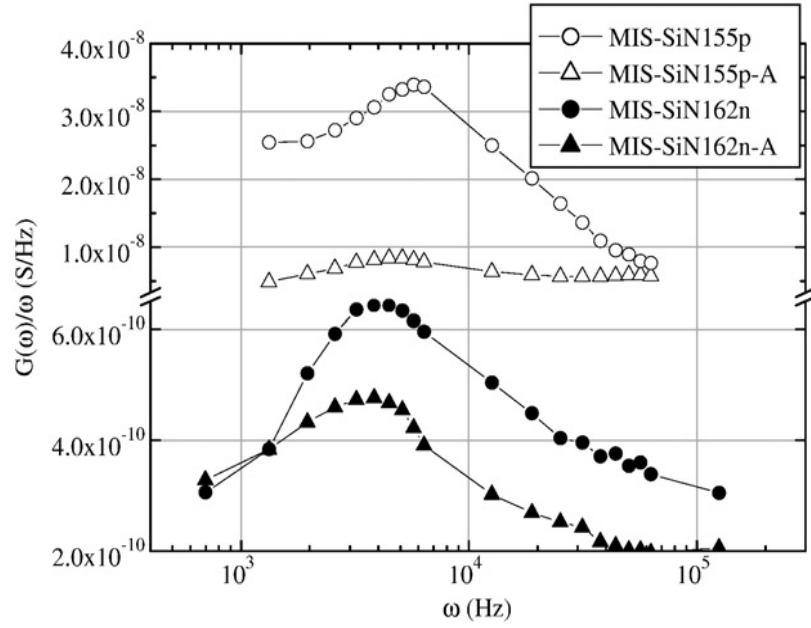
In Si solar cell devices,  $\text{SiN}_x$  layer which is deposited on  $n^+$  emitter layer acts as both passivation layer and anti reflection coating (ARC). It is observed that there is degradation in cell parameters when a Si solar cell is soaked under UV light illumination. Figure 4.1 shows the variation in solar cell parameters with light exposure time. It is seen that the conversion efficiency decreased by 0.5% after light soaking and this loss is due to the increase in interface trap density ( $D_{it}$ ) from  $2.8 \times 10^{11}$  to  $4.2 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$  at the a-Si:H/Si interface.<sup>7</sup> The interface trap states are due to silicon dangling bonds which consist of a silicon atom bonded to three nitrogen atoms, having an unpaired electron. It is also seen that the interface trap density is higher for p-type wafers compared to that of n-type as shown in Figure 4.2.<sup>7</sup> Thus, the degradation will be more for devices fabricated on p-Si in comparison to devices fabricated on n-Si wafer. Figure 4.3 shows that there is a decrease in  $D_{it}$  (recovery occurs) when the wafer is annealed at  $350^\circ\text{C}$  for 20 mins.<sup>8</sup>



**Figure 4.1** Variation in photovoltaic parameters during UV light exposure.<sup>7</sup>



**Figure 4.2**  $G(\omega)/\omega$  vs.  $\omega$  for samples on p and n wafers.<sup>7</sup>



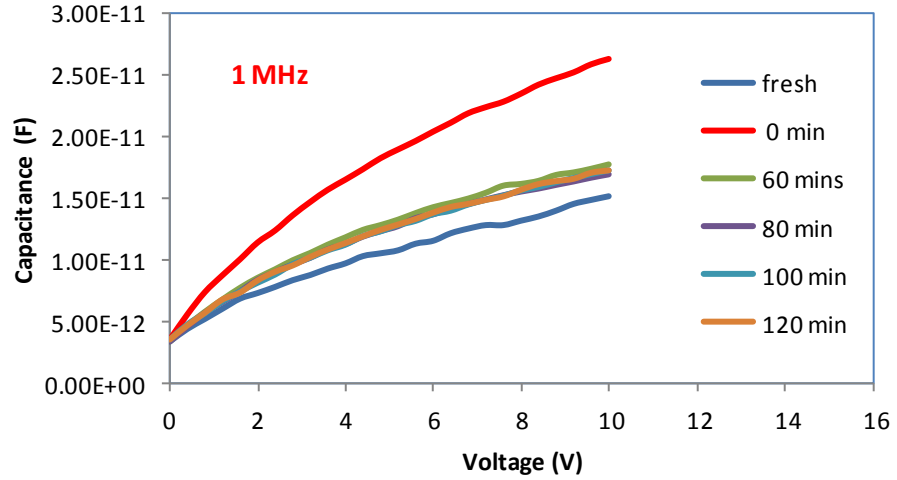
**Figure 4.3**  $G(\omega)/\omega$  vs.  $\omega$  for samples on p- and n wafers before and after annealing at 350°C for 20 mins.<sup>8</sup>

## 4.2 Experimental

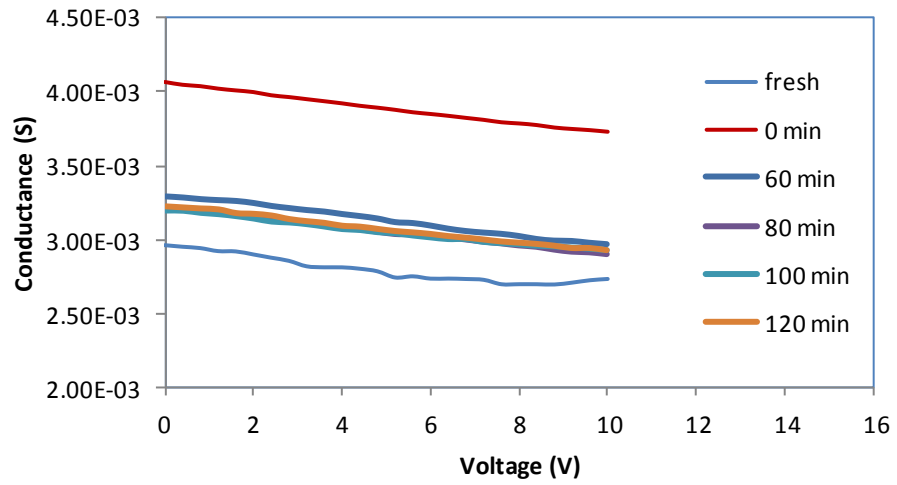
Monocrystalline Si solar cells of area  $< 1 \text{ cm}^2$  were soaked for about 5 hrs duration. The temperature of the chuck of the diode prober increases to 37°C during this soaking. The lamp is switched off after light soaking and both C-V and G-V measurements of the entire cell are measured after different time intervals. The C-V and G-V characteristics are shown in Figure 4.4.

### C-V of 5 hrs light soaked sample

Measurements are taken after different time intervals after light is turned off

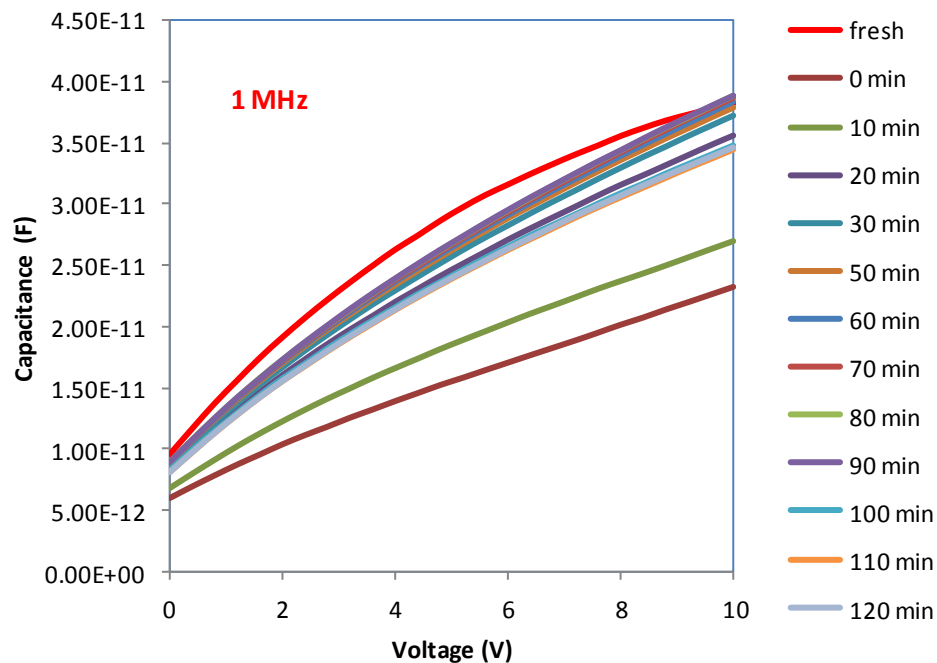


(a)

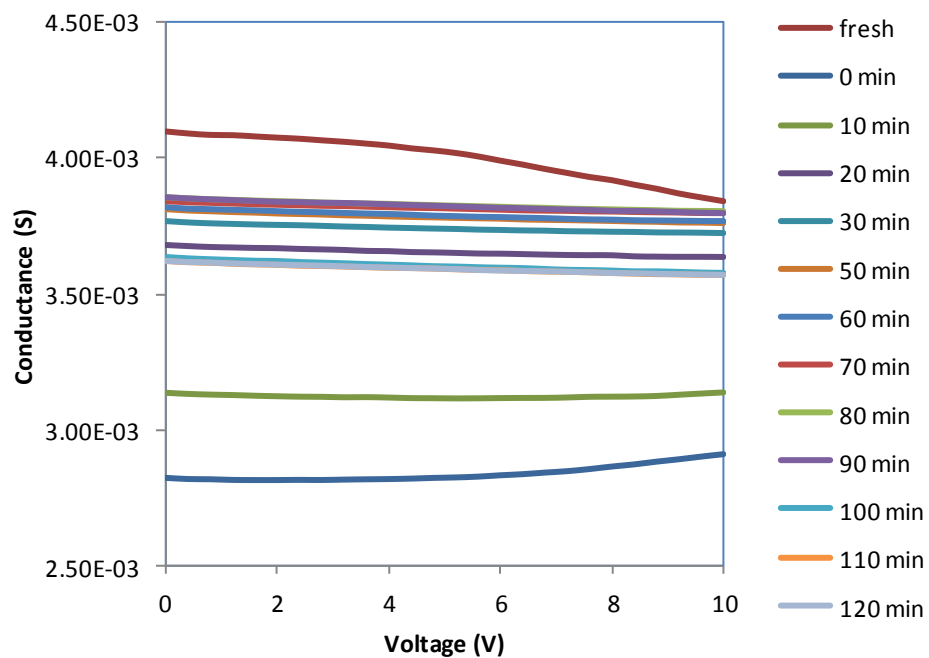


(b)

**Figure 4.4** (a) C-V and (b) G-V characteristics after 5 hrs light soaking of a larger sample.

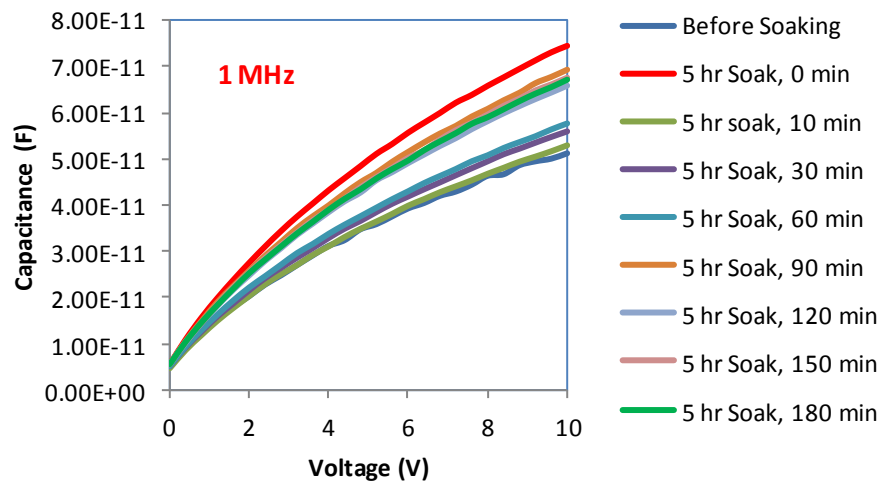


(a)

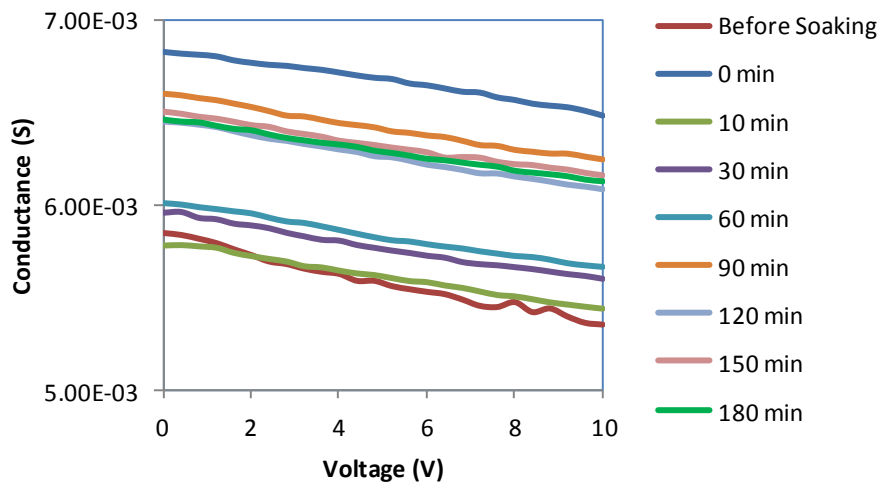


(b)

**Figure 4.5** (a) C-V and (b) G-V characteristics of a smaller sample.

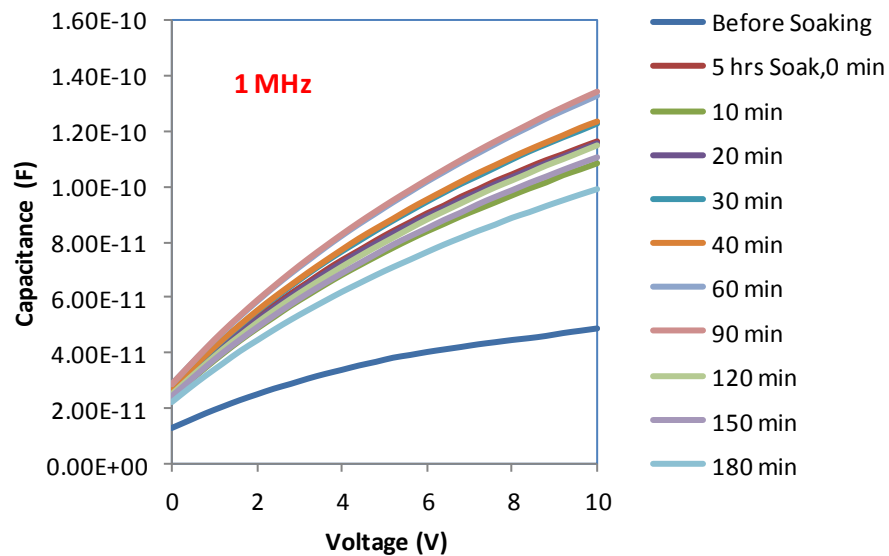


(a)

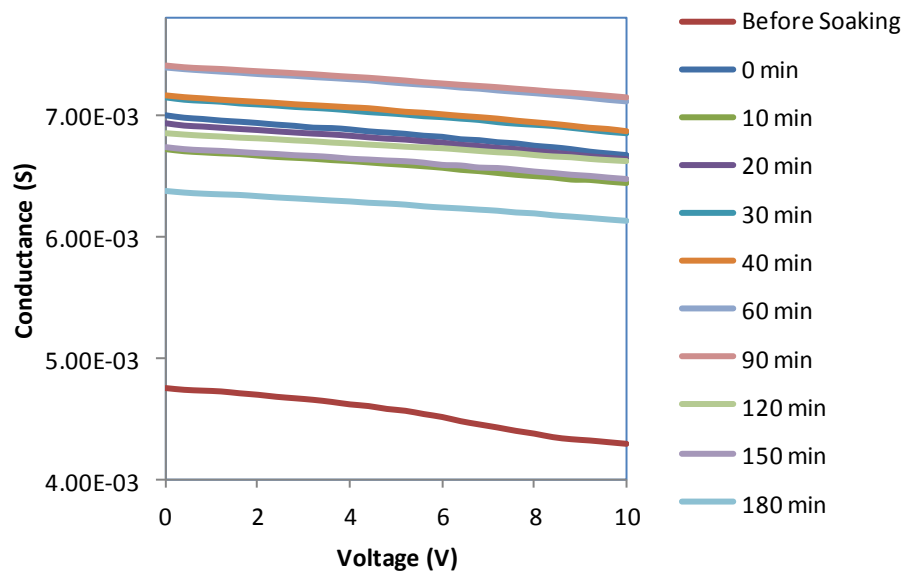


(b)

**Figure 4.6** Repeated (a) C-V and (b) G-V measurements on larger sample shown in Figure 4.4.



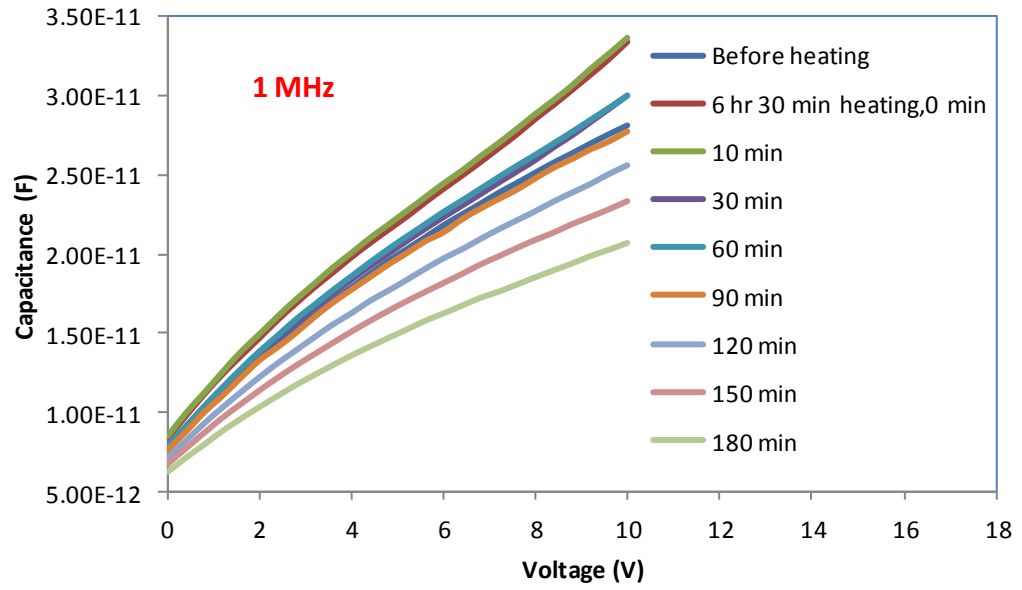
(a)



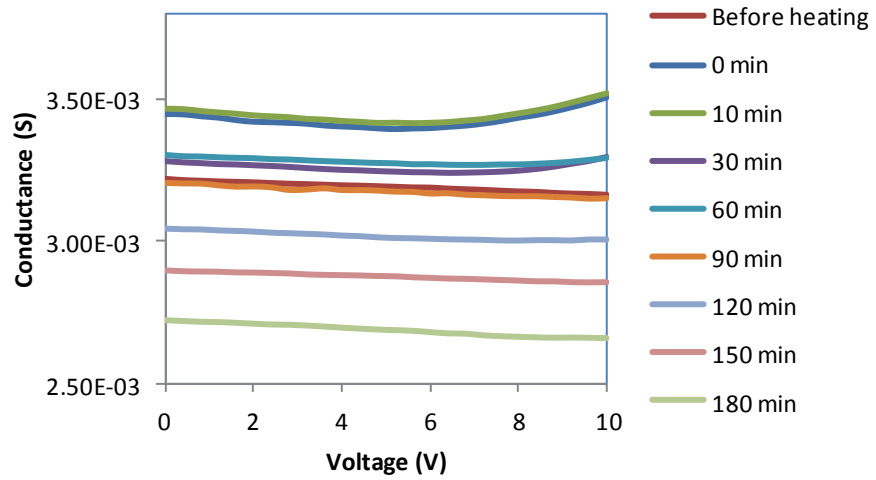
(b)

**Figure 4.7** Repeated (a) C-V and (b) G-V measurements on smaller sample shown in Figure 4.5.



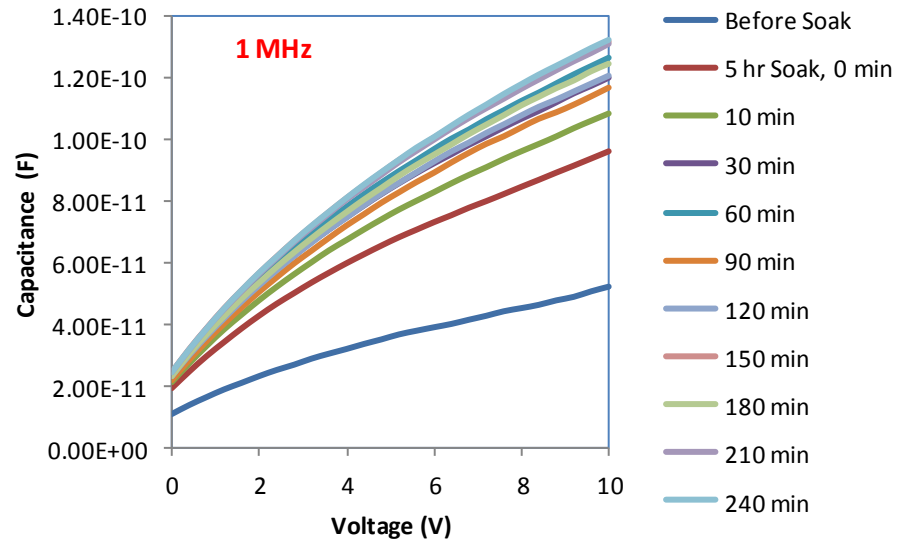


(a)

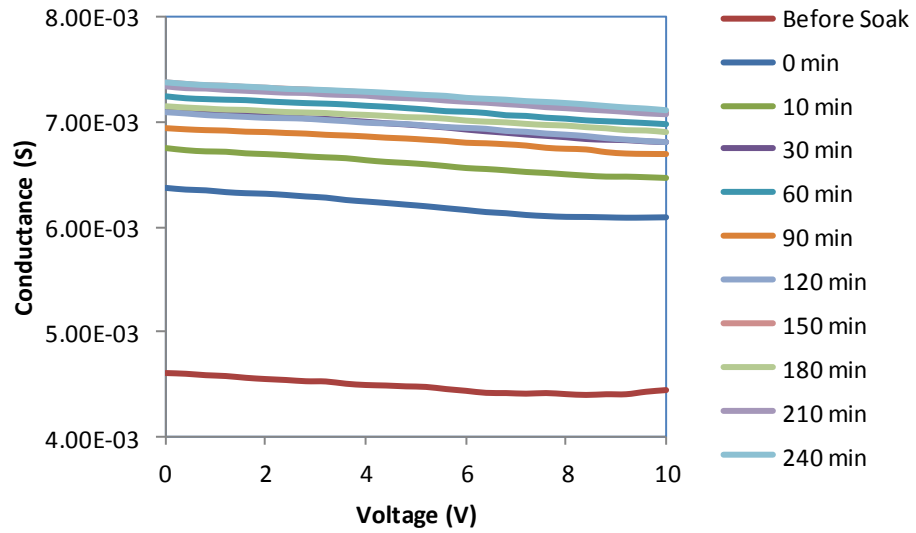


(b)

**Figure 4.8** Repeated (a) C-V and (b) G-V measurements on smaller sample showing heating effect.



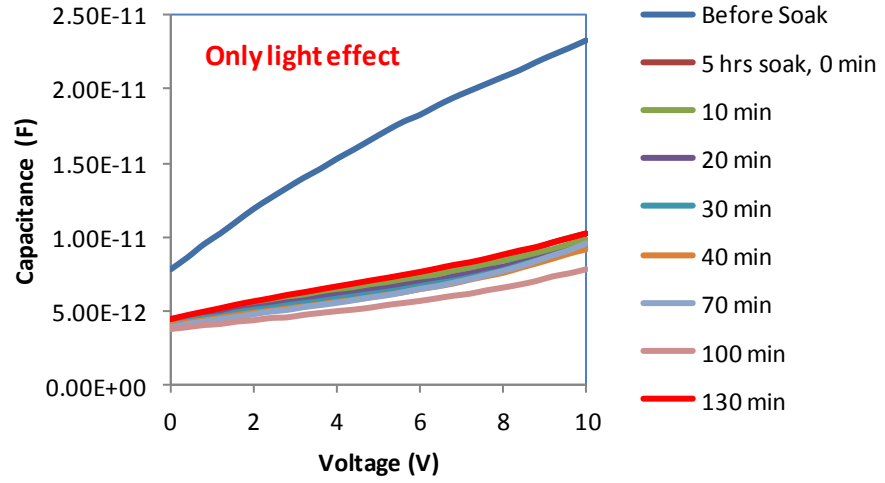
(a)



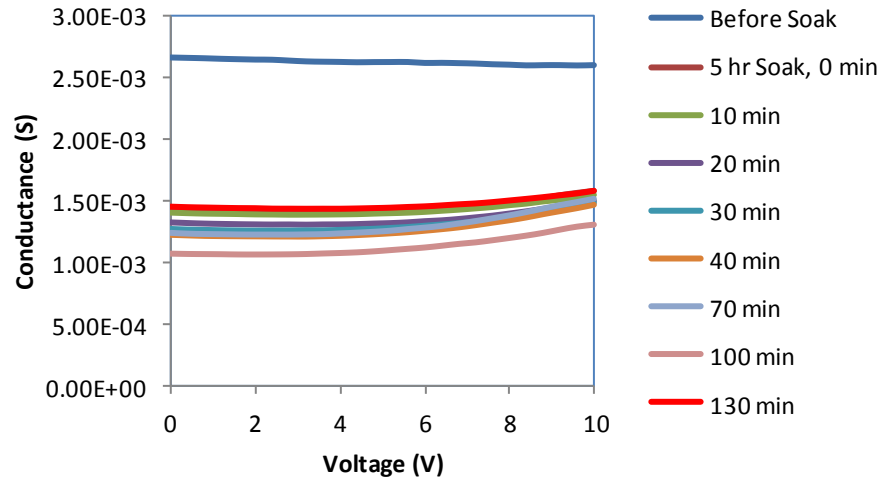
(b)

**Figure 4.9** Repeated (a) C-V and (b) G-V measurements on smaller sample shown in Figure 4.5.

### Light Effect Only

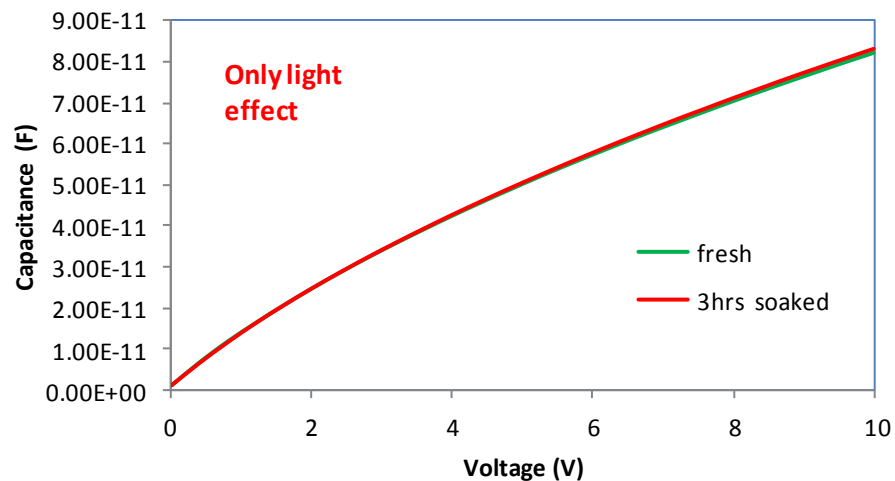


(a)

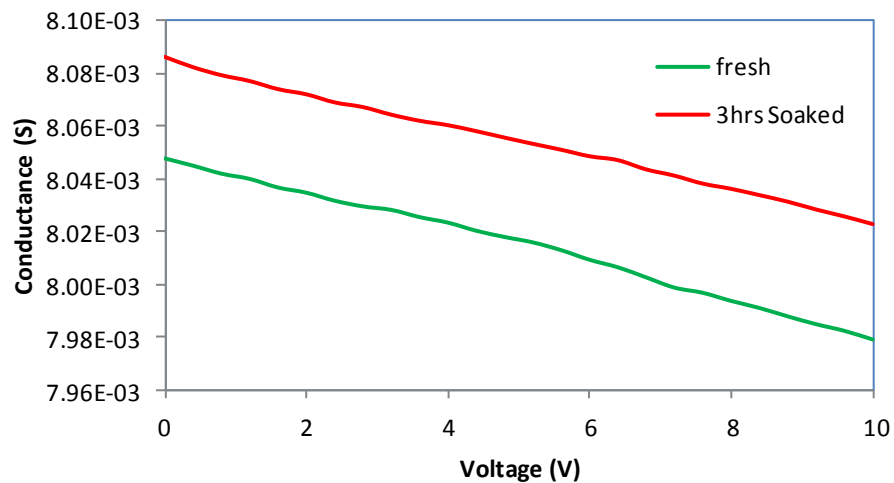


(b)

**Figure 4.10** (a) C-V and (b) G-V measurements of sample 1 (smaller) after 5 hrs light soaking.

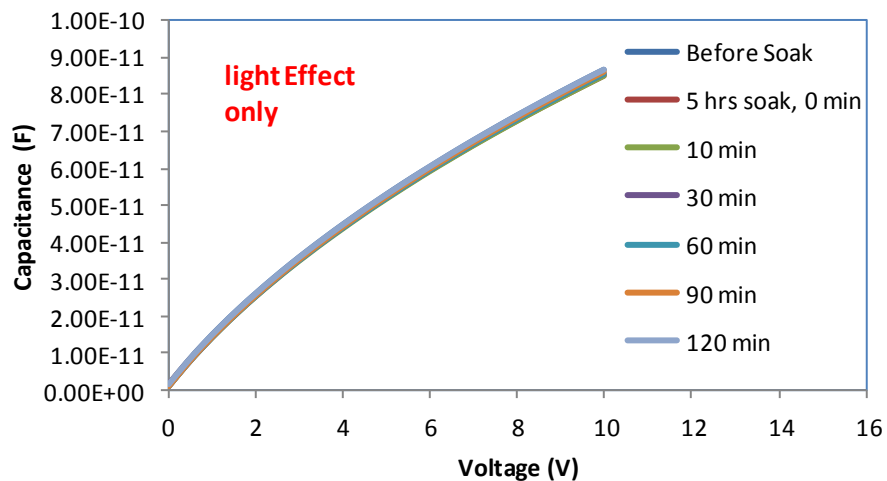


(a)

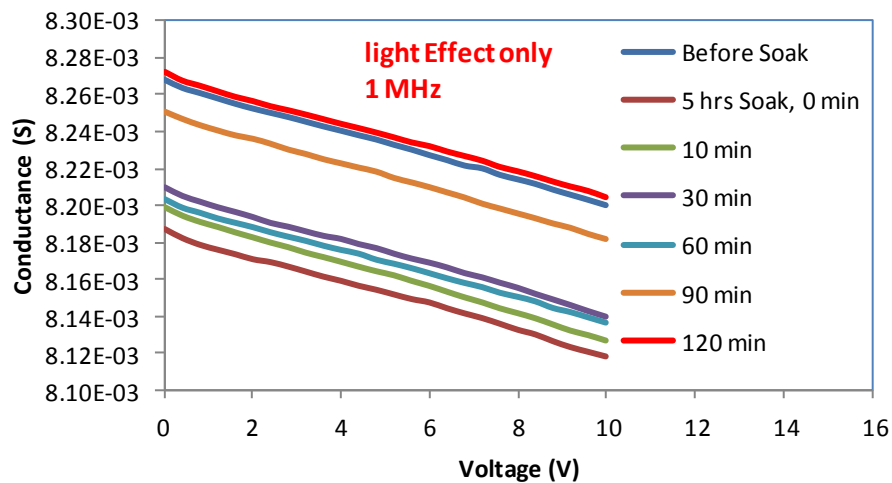


(b)

**Figure 4.11** (a) C-V and (b) G-V measurements of sample 2 (larger) after 3 hrs light soaking (lamp fused after some time).

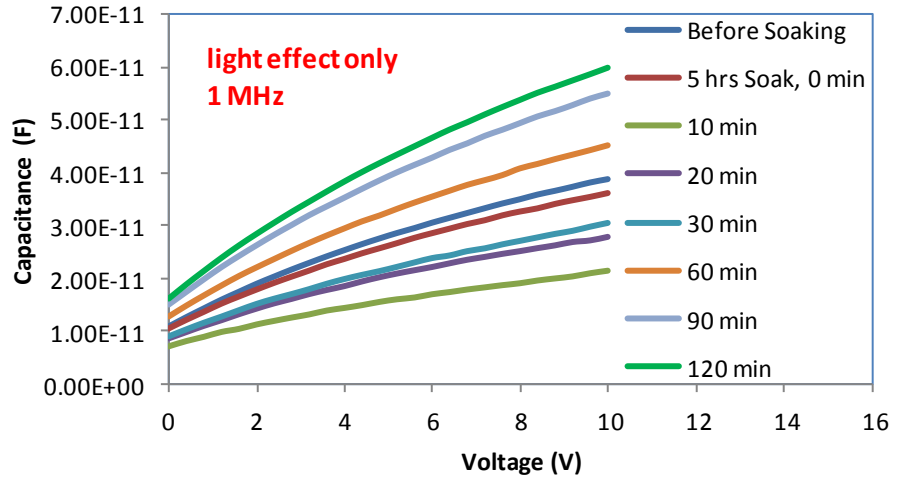


(a)

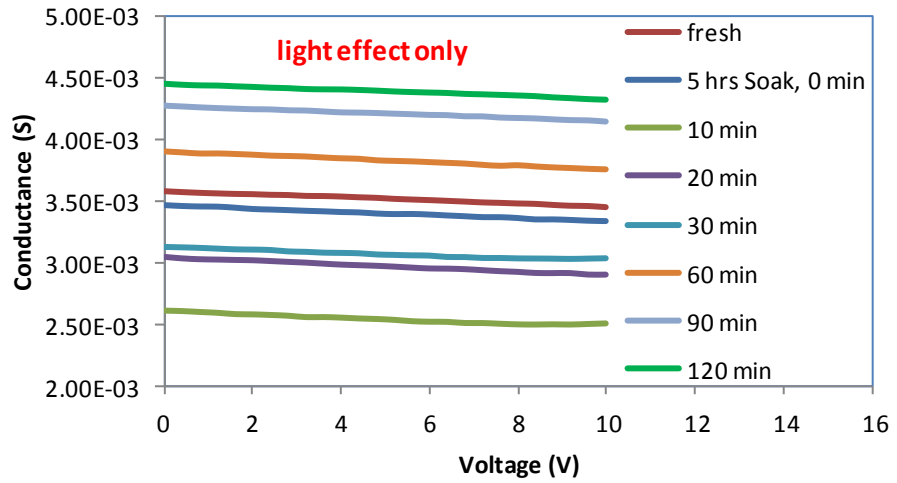


(b)

**Figure 4.12** (a) C-V and (b) G-V characteristics of sample 2 (larger) repeated after 5 hrs light soaking.



(a)



(b)

**Figure 4.13** (a) C-V and (b) G-V characteristics of sample 1 (smaller) (repeated) after 5 hrs light soaking.

### Results and Discussion

From the light soaking experiments, it is observed that there is increase in both C-V and G-V characteristics of the entire Si solar cell after 5 hrs of soaking under light compared to fresh device. Thus, there is an increase in interface trap density ( $D_{it}$ ) at the  $\text{SiN}_x/\text{n}^+$  interface after soaking.

## CHAPTER 5

### CONSTANT VOLTAGE STRESS (CVS) INDUCED DEGRADATION

#### 5.1 Constant Voltage Stress (CVS)

In constant voltage stressing (CVS), a particular voltage is applied for a certain interval of time to the gate terminal of the  $\text{Cu/SiN}_x/\text{n}^+$  MOS capacitor. When a positive bias (+ 10V) is applied to the gate (Cu) terminal, electrons will flow from the  $\text{n}^+$  layer through the  $\text{SiN}_x$  passivation layer towards the gate. During the transport of electrons through the  $\text{SiN}_x$ , they will break the Si-H bonds present at the  $\text{SiN}_x/\text{n}^+$  interface. As a result, Si dangling bonds will be created at the interface. These Si dangling bonds contribute to the interface trap states at the interface. These interface states will influence the performance of the Si solar cells. It is observed that the  $\text{SiN}_x$  dielectric layer causes instabilities in threshold voltage in thin film transistors (TFT) due to constant voltage stressing. It is believed that the CVS will degrade the  $\text{SiN}_x/\text{n}^+$  interface and the generated interface trap states ( $D_{it}$ ) will affect the Si solar cell performance parameters.

#### 5.2 Introduction

Nowadays, it is well known that c-Si solar cells fabricated on Czochralski (CZ) wafers exhibit light-induced degradation (LID) of the cell parameters.<sup>9,10</sup> Generally, this effect is ascribed to boron-oxygen (B-O) defect complex which is formed in the wafer itself due to prolonged exposure of CZ wafers to light.<sup>11</sup> As a finished Si solar cell has a multilayered

structure, it is also possible to have some degradation at various interfaces upon light illumination. The study of degradation mechanism is, therefore, important in Si solar cell devices. The anti reflection coating (ARC) of SiN:H layer on  $n^+$  region, an integral part of Si solar cells, can contribute to the degradation process. In particular, it is recognized that the SiN:H/Si interface has trap states in the form of interface states and a strong positive charge accumulation, at the interface, can be affected by light exposure.<sup>12</sup> Recently, it was also reported that there is an increase in the interface trap density ( $D_{it}$ ) upon light soaking whereas it decreases with annealing.<sup>7,8</sup> So far, most of the studies are performed on a regular MOS capacitor device in order to determine the changes in the density of interface trap states due to light exposure or thermal annealing. However, in a regular Si solar cell, the effect of the SiN:H dielectric layer on solar cell parameters will be different upon light soaking when compared to an MOS capacitor. In addition, the effect of SiN:H/ $n^+$  interface on the cell performance parameters of Si solar cells has not yet been studied in detail.

In this work, the interface trap states at the SiN:H/ $n^+$  interface and their variation due to constant voltage stress (CVS), applied across the Cu/SiN:H/ $n^+$  MOS capacitor, in a multicrystalline Si solar cell device have been studied. It is observed that there is degradation at the interface of SiN:H/ $n^+$  of the MOS capacitor whereas no significant change is seen at the  $n^+$ /p junction due to CVS. It is further observed that the interface degradation of SiN:H/ $n^+$  of the MOS capacitor directly affects the solar cell performance.



### 5.3 Experimental

In order to investigate the effect of constant voltage stressing (CVS), multicrystalline (mC) Si solar cells of smaller dimensions have been used. Solar cells of area  $<1 \text{ cm}^2$  were taken for the study of device degradation due to CVS. A copper probe with circular tip of 1 mm in diameter was used as the top contact for the electrical measurements. A constant voltage stress of + 10V was applied to the top contact (Cu) of Cu/SiN:H/n<sup>+</sup>-Si MOS capacitor of area  $0.008 \text{ cm}^2$  for various stress times at room temperature. Current-voltage (I-V) and capacitance-voltage (C-V) (at 10 kHz) measurements for both MOS capacitor and junction diode ( $\sim 0.5 \text{ cm}^2$  in area) were taken for fresh and stressed devices using Keithley 238 high current source measure unit and HP 4284A precision LCR meter respectively. All the electrical characterization were carried out using a 680A semi-automatic diode prober.

### 5.4 Results and Discussion

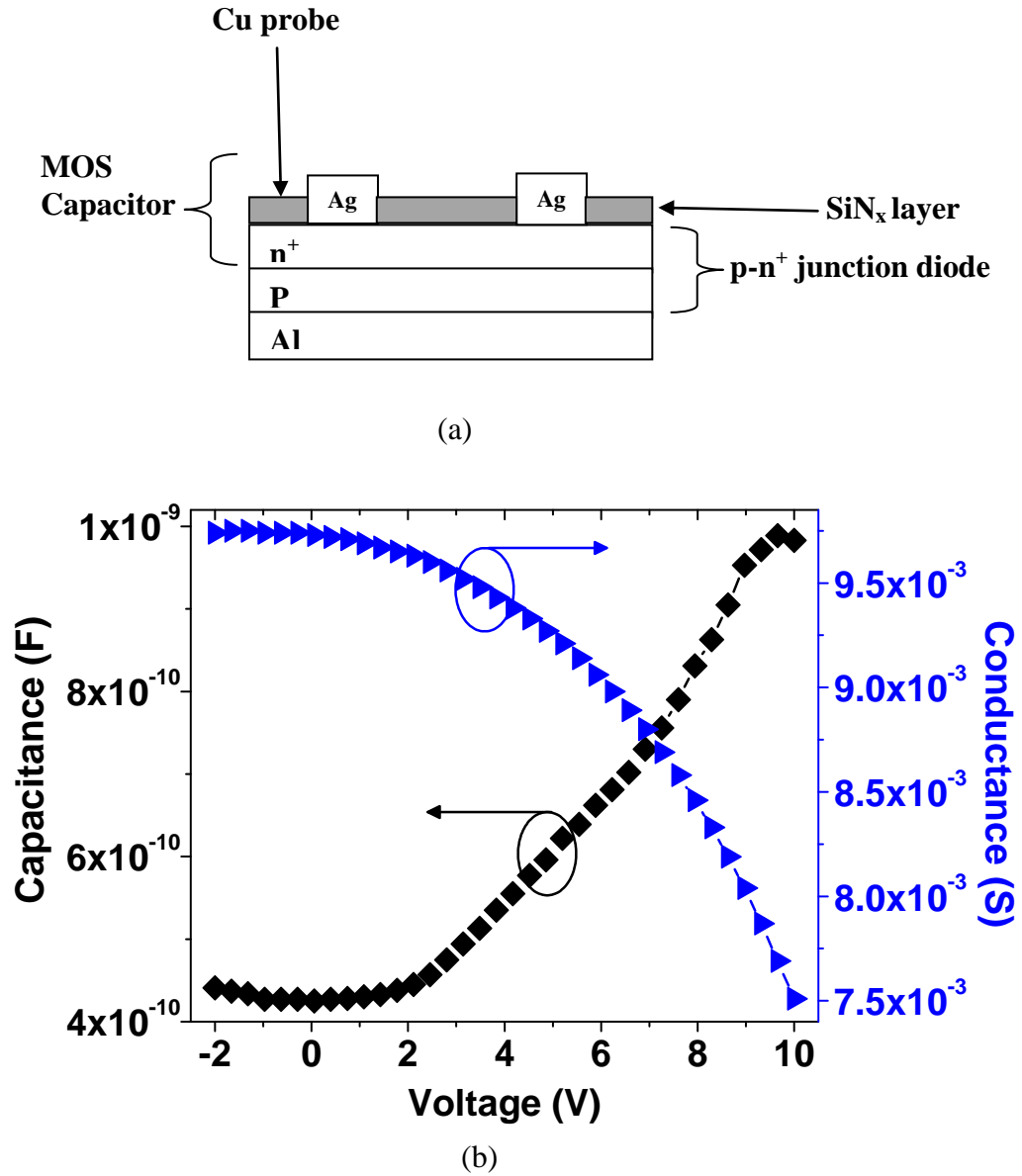
Figure 5.1(a) shows the cross-sectional view of the Si solar cell device which is used in this work. The structure consists of a p-n<sup>+</sup> junction diode and Cu/SiN:H/n<sup>+</sup> MOS capacitor. Figure 5.1(b) shows the C-V and conductance-voltage (G-V) characteristics for a fresh Cu/SiN:H/n<sup>+</sup> MOS capacitor. From the plots, it can be seen that there is a significant amount of interface trap states already present at the SiN:H/n<sup>+</sup> interface. The interface trap density ( $D_{it}$ ) can be calculated using conductance method and is given by<sup>13</sup>,

$$D_{it} = \frac{2.5}{q} \left( \frac{G_p}{\omega} \right)_{\max} \quad (5.1)$$

where,  $G_p$  is the parallel conductance and is given by<sup>14</sup>,

$$G_p = \frac{\omega^2 G_m C_{dielectric}^2}{a (G_m^2 + \omega^2 (C_{dielectric} - C_m)^2)} \quad (5.2)$$

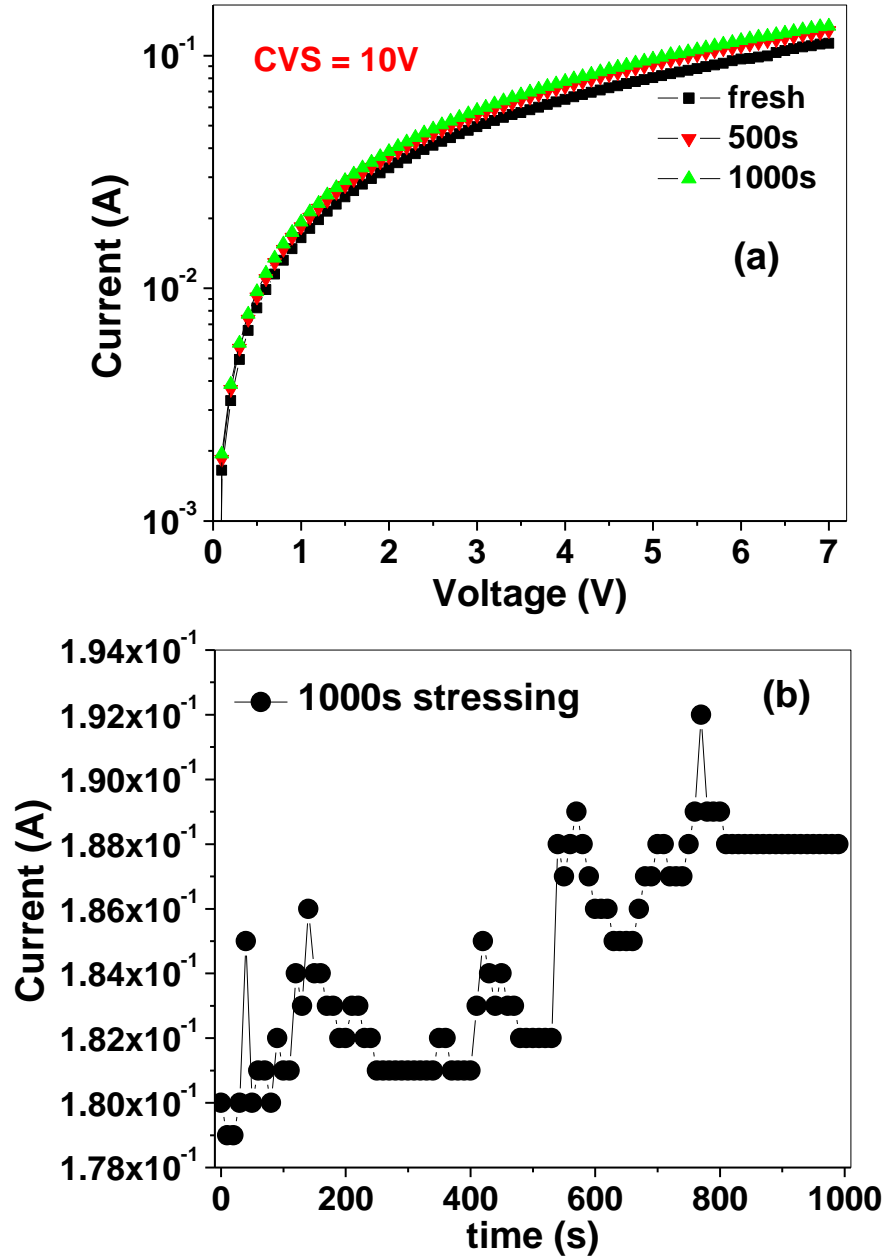
where,  $a$  is the area of the top electrode,  $\omega = 2\pi f$ ,  $C_{dielectric}$  is the accumulation capacitance,  $C_m$  and  $G_m$  are the measured capacitance and conductance respectively. The calculated value of  $D_{it}$  for the fresh MOS capacitor in a regular Si solar cell device, is  $2.64 \times 10^9 \text{ cm}^{-2} \text{ eV}^{-1}$  which is close to the reported value of  $\sim 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ , obtained on a normal MOS capacitor with an  $n^+$  substrate.<sup>7</sup> A Si solar cell is a complicated device containing p- $n^+$  junction diode beneath the SiN:H MOS capacitor. There is every possibility that the interface trap density ( $D_{it}$ ), at the SiN:H/ $n^+$  junction, can affect the junction diode performance. The impact of SiN:H/ $n^+$ -Si interface degradation on solar cell performance has been evaluated by applying a constant voltage stress (CVS) on the Cu/SiN:H/ $n^+$  MOS capacitor.



**Figure 5.1** Cross-sectional view of the Si solar cell device showing n<sup>+</sup>/p junction diode and SiN<sub>x</sub> MOS capacitor (a) and C-V and G-V characteristics of Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor at 10 kHz for fresh device (b).

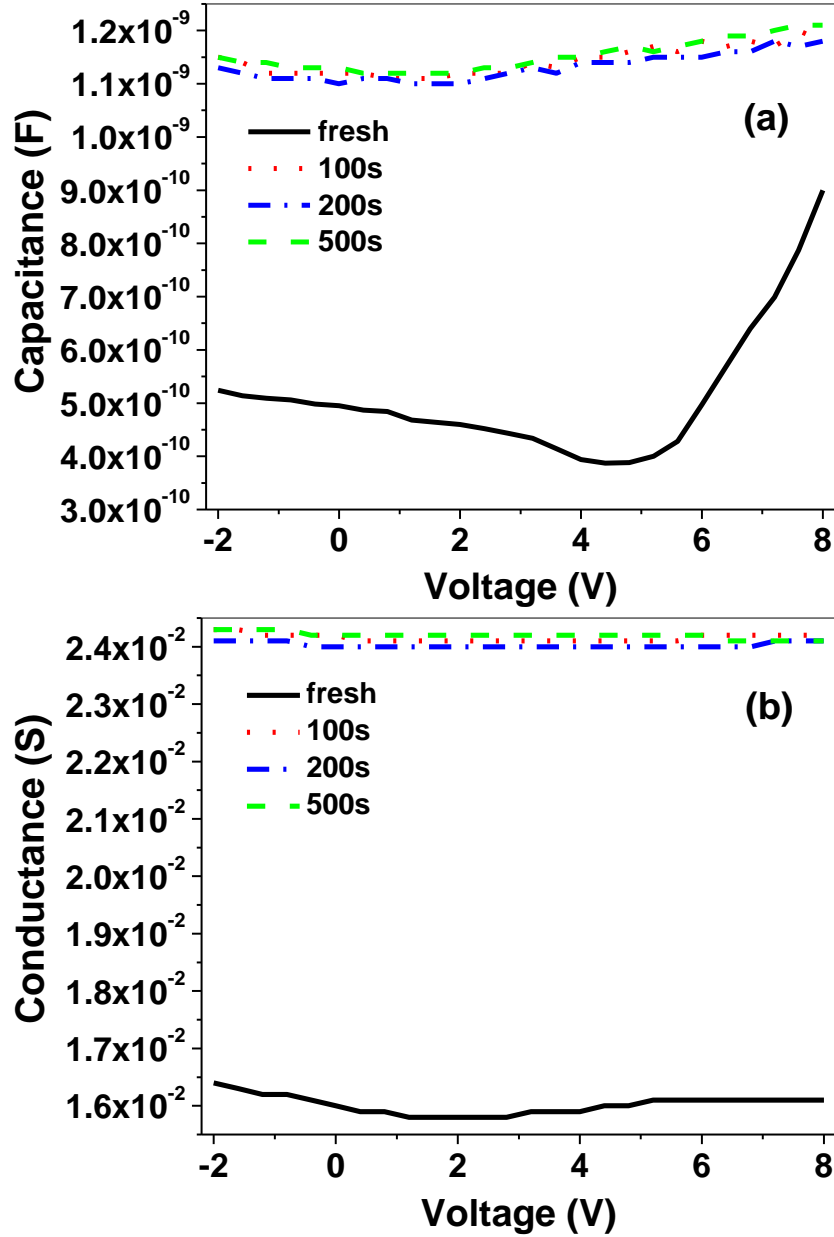
Figure 5.2 (a) shows the I-V characteristics for fresh and stressed devices after CVS of +10 V on the SiN<sub>x</sub> MOS capacitor. It is observed that the leakage current of stressed devices is higher than that of fresh devices and increases with the increase in stress time. The stress induced leakage current (SILC) of Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor is

mostly due to the creation of traps at the  $\text{SiN}_x/\text{n}^+$  interface and in the bulk of the  $\text{SiN}_x$  during CVS.<sup>15</sup> Figure 5.2 (b) shows the increase in leakage current as a function of stress during a 1000-s stress. This is consistent with the stress-induced defect formation at the interface.

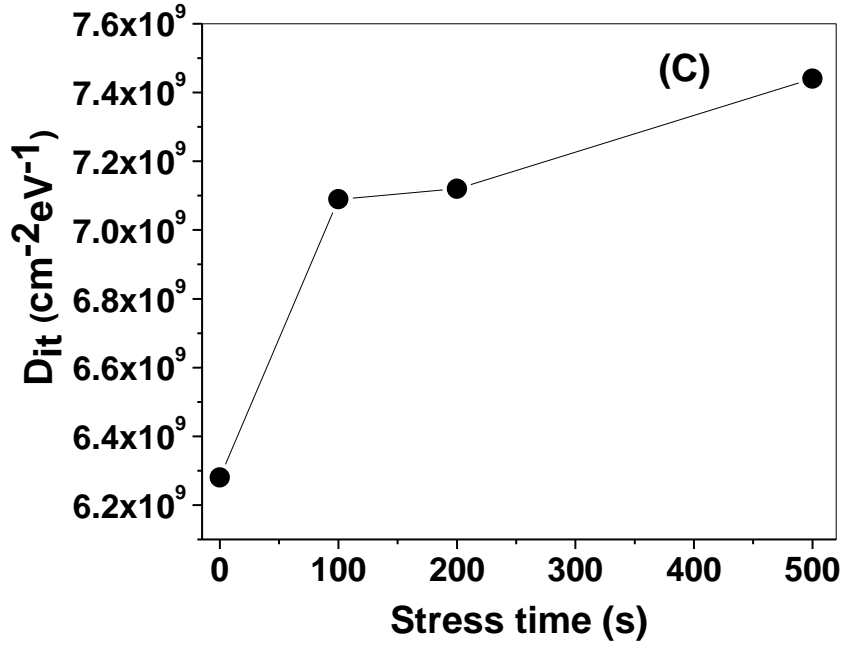


**Figure 5.2** (a) I-V characteristics of Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor for various stressing times for CVS at 10V and (b) I-t plot showing the current increase as a function of stress time.

The antireflection coating (ARC) consists of hydrogenated SiN (SiN:H) layer containing Si-H bonds. The constant voltage stress, applied to this SiN:H layer, will rupture the Si-H bonds creating Si dangling bond (Si DB) defects which contribute to the interface trap states at the SiN:H/ $n^+$  interface. Therefore, the density of interface trap states ( $D_{it}$ ) increases with stress time as more number of Si dangling bonds are created due to CVS.



**Figure 5.3** (a) C-V and (b) G-V characteristics of Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor at 10 kHz for various stressing times and  $D_{it}$  versus stress time (c) for CVS at 10V.

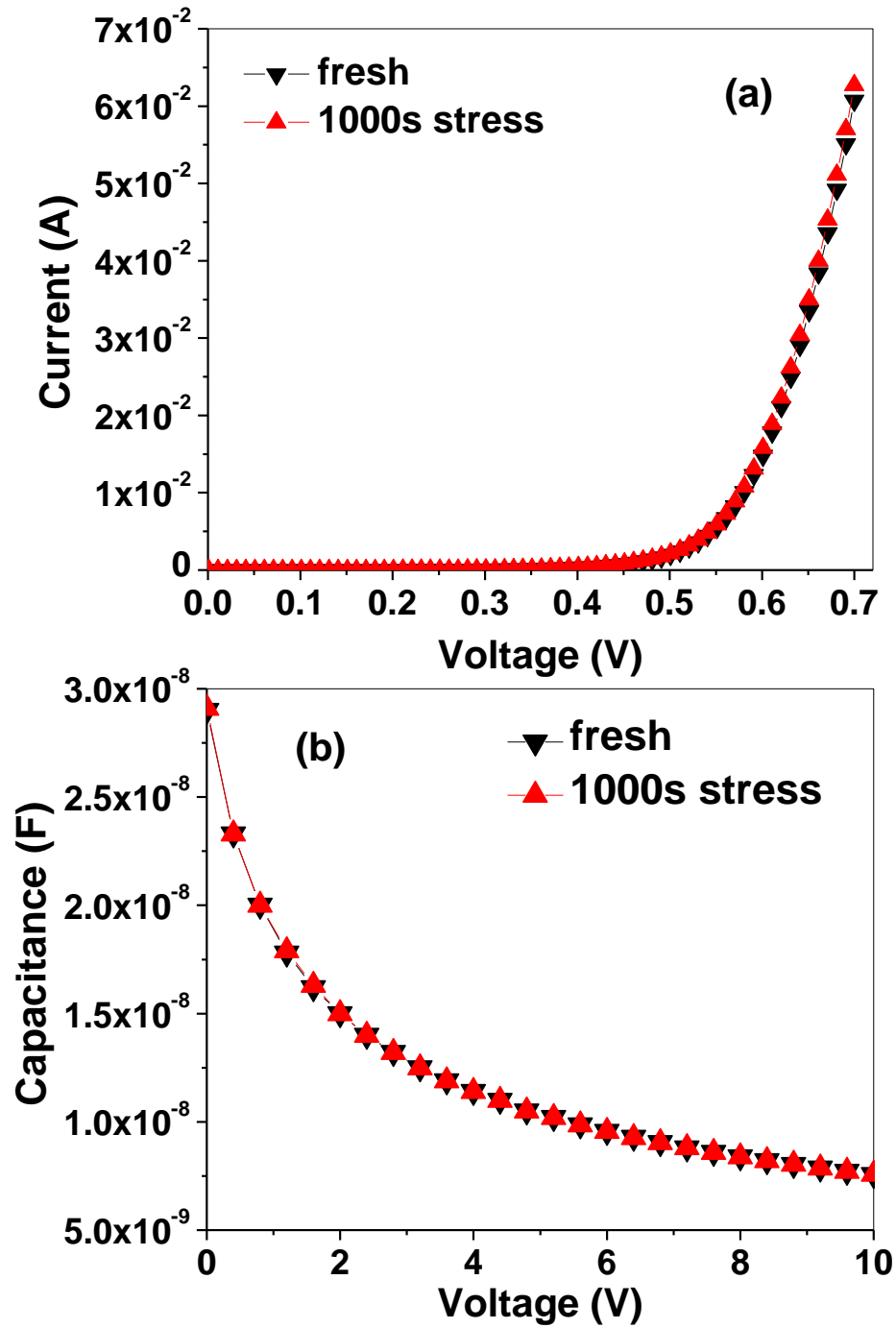


**Figure 5.3** (a) C-V and (b) G-V characteristics of Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor at 10 kHz for various stressing times and  $D_{it}$  versus stress time (c) for CVS at 10V. Continued.

Figures 5.3 (a) and (b) show the C-V and G-V characteristics, respectively, for the Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor for fresh and stressed devices. It is seen that there is a change in capacitance and conductance for the stressed devices as compared to that of the fresh devices and this increment is due to the generation of more interface trap states at the SiN<sub>x</sub>/n<sup>+</sup> interface. It is also observed that, as the stressing time increases, both capacitance and conductance characteristics are severely degraded. This is because of an increase in interface trap states. The variation in interface trap density ( $D_{it}$ ) with stress time is shown in Figure 5.3 (c). The observed increase in  $D_{it}$  values clearly suggests the creation of interface trap states by CVS.

Figure 5.4 (a) shows the I-V characteristics for fresh and 1000s stressed p-n<sup>+</sup> junction diode at CVS of 10V. No significant change in the I-V characteristics was observed after constant voltage stress of the SiN<sub>x</sub> MOS capacitor indicating that the

junction diode characteristics were not affected during stress. Figure 5.4 (b) shows the C-V characteristics measured at a frequency of 10 kHz for the p-n<sup>+</sup> junction diode before and after 1000s stress at 10V. The C-V plots for the p-n<sup>+</sup> junction diode



**Figure 5.4** (a) Dark I vs. V and (b) C vs. V characteristic at 10 kHz of p-n<sup>+</sup> junction diode before and after stressing for CVS at 10V.

remained unchanged due to the constant voltage stressing applied to the Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor. The depletion region of p-n<sup>+</sup> junction diode, therefore, remained damage free even after the 1000s stress.

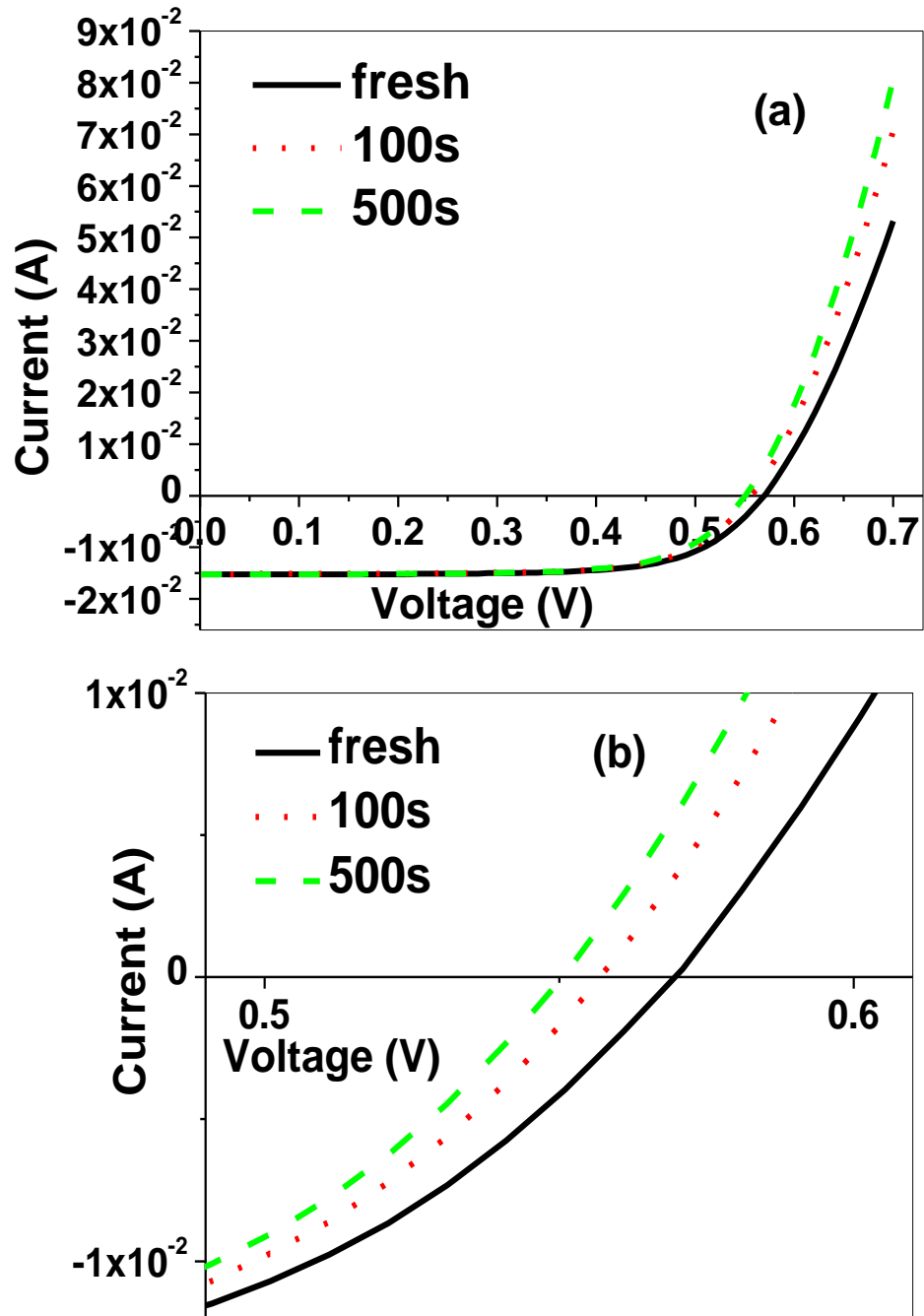
Figure 5.5 (a) shows the I-V characteristics under 1-sun illumination at room temperature of p-n<sup>+</sup> junction diode for fresh and stressed devices after CVS of 10V for different stress times. It is observed that the illuminated I-V plots intersect the voltage axis at various points for different stress times indicating a decrease in open-circuit voltage ( $V_{oc}$ ) from 570 to 550 mV as the stress time increases. Since there is no additional defects in the depletion layer, the observed degradation in  $V_{oc}$  is mainly due to the increase in interface trap density ( $D_{it}$ ) at the SiN<sub>x</sub>/n<sup>+</sup>-Si interface during stress (Figure 5.3(c)). No significant change in  $I_{sc}$  is observed with stress time whereas the conversion efficiency ( $\eta$ ) decreased from 12.1 to 11.6% due to an increase in  $D_{it}$  from  $6.3 \times 10^9$  to  $7.5 \times 10^9 \text{ cm}^{-2}\text{eV}^{-1}$  with stress times as  $V_{oc}$  decreases. An illuminated solar cell generates electron-hole pairs, which diffuse towards the interface. The carriers reaching the SiN<sub>x</sub>/n<sup>+</sup>-Si interface can experience surface recombination due to interface trap states, and are lost during the power-generation process.<sup>12,2</sup> The recombination rate ( $U_s$ ) due to interface trap states is given by<sup>12,16</sup>,

$$U_s = (n_s \cdot p_s - n_i^2) \cdot v_{th} \int_{E_v}^{E_c} \frac{D_{it}(E_t)}{\frac{(n_s + n_1)}{\sigma_p(E_t)} + \frac{(p_s + p_1)}{\sigma_n(E_t)}} dE_t, \quad (5.3)$$

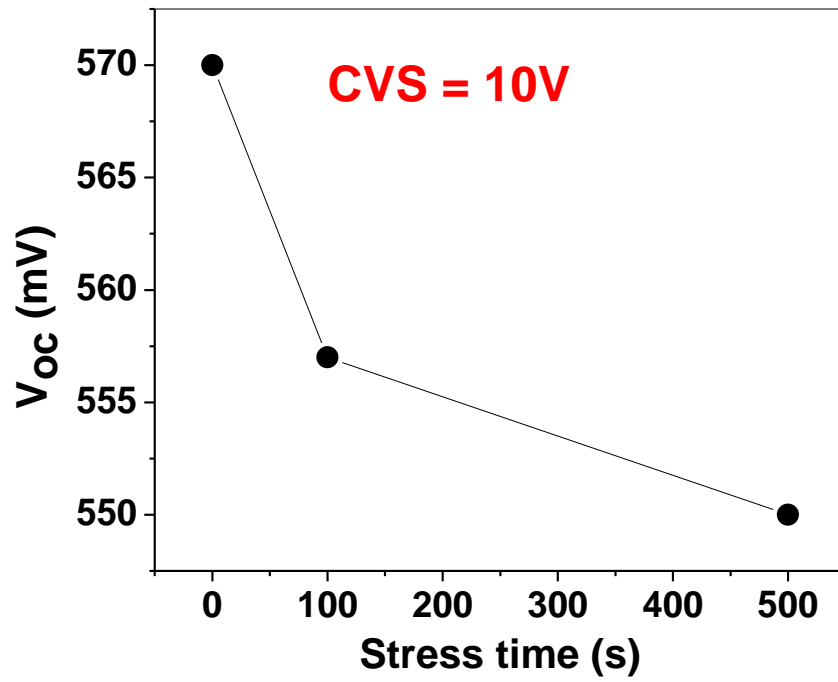
where,  $D_{it}$  is the interface trap density,  $E_t$  is the trap level energy,  $\sigma_n$  and  $\sigma_p$  are the electron and hole capture cross-sections respectively,  $v_{th}$  is the thermal velocity,  $n_s$  and  $p_s$  are the electron and hole concentrations at the surface respectively and  $n_1$  and  $p_1$  depend on the energy of the defect level within the forbidden gap. It is seen from (Eq. (5.3)) that



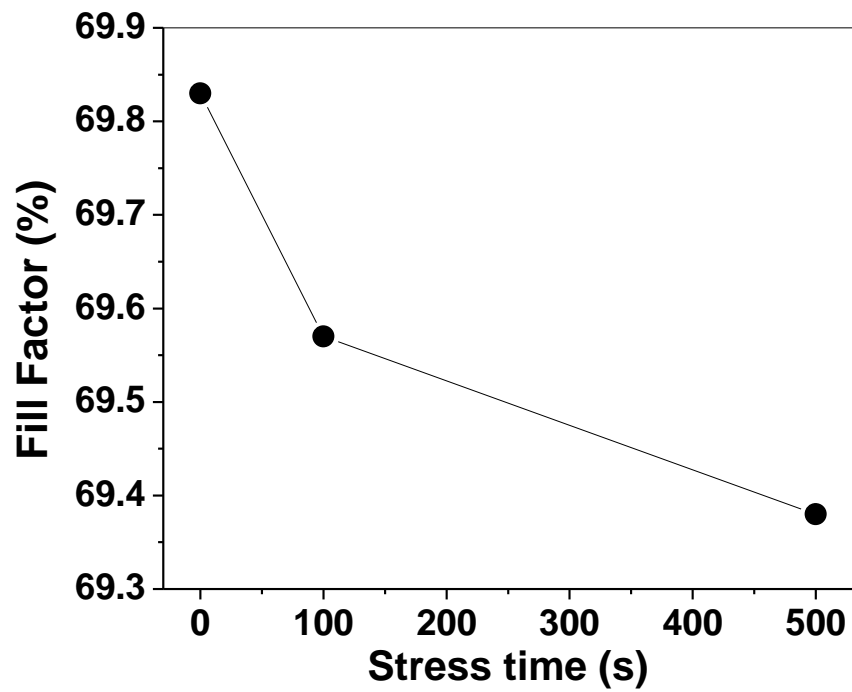
the recombination rate is strongly dependent on the interface trap density ( $D_{it}$ ). Therefore, the recombination rate increases as  $D_{it}$



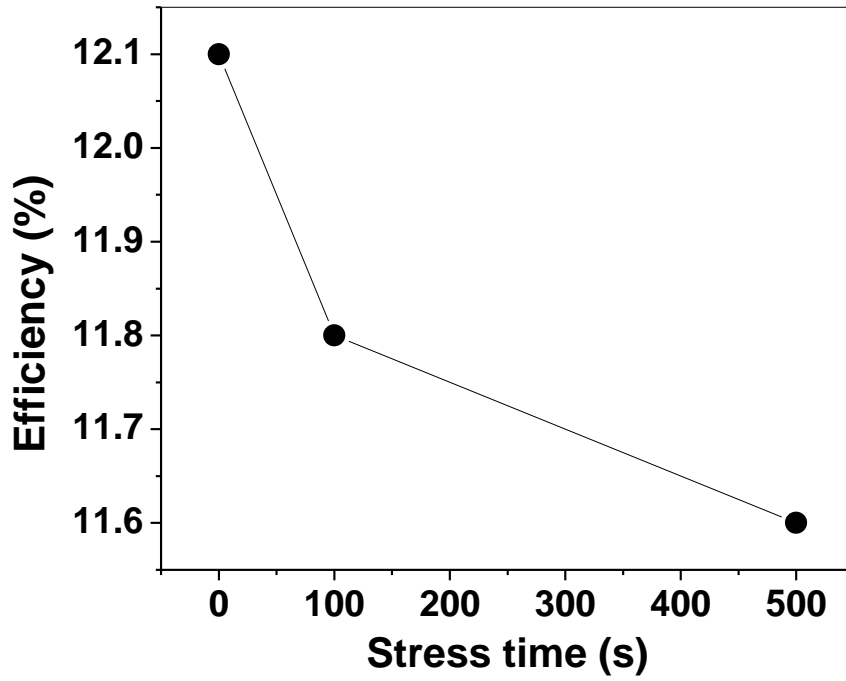
**Figure 5.5** (a) Light I-V characteristics of p-n<sup>+</sup> junction diode before and after stressing for CVS at 10V and (b) shows the light I-V characteristics in the enlarged form of the region where the plots intersect the x-axis.



**Figure 5.6** Short-circuit voltage ( $V_{oc}$ ) vs. stress time for Si solar cell for CVS at 10V.



**Figure 5.7** Fill factor (FF) vs. stress time for Si solar cell for CVS at 10V.



**Figure 5.8** Conversion Efficiency ( $\eta$ ) vs. stress time for Si solar cell for CVS at 10V.

increases. Hence, more carriers are lost due to recombination. The shift in the illuminated I-V characteristics and degradation is, therefore, observed in solar cell performance parameters due to CVS. Thus,  $D_{it}$  formed at the  $\text{SiN}_x/\text{n}^+\text{-Si}$  interface, either by stress (as in this case) or during cell fabrication, has a direct correlation with the degradation of the cell performance. Therefore, the application of CVS on the  $\text{Cu/SiN}_x/\text{n}^+$  MOS capacitor of area  $0.008 \text{ cm}^2$  creates a big impact on the Si solar cell with  $0.5 \text{ cm}^2$  in area and there is a decrease in conversion efficiency by  $\sim 4.13\%$ .

Figures 5.6 and 5.7 show the variation in open-circuit voltage ( $V_{oc}$ ) and fill factor (FF), respectively, with stress time whereas Figure 5.8 shows conversion efficiency versus stress time. It is observed that  $V_{oc}$ , FF, and efficiency decrease with stress time due to the increase in interface trap density ( $D_{it}$ ).

## 5.5 Conclusions

In summary, a constant voltage stress (CVS) of +10 V is applied, for different stress times, to the Cu/SiN<sub>x</sub>/n<sup>+</sup>-Si MOS capacitor to simulate the effects of SiN<sub>x</sub>/n<sup>+</sup>-Si interface degradation on Si solar cell performance characteristics. Significant shifts in I-V, C-V, and G-V characteristics of SiN<sub>x</sub> MOS capacitor were observed demonstrating an increase in interface trap density across the SiN<sub>x</sub>/n<sup>+</sup>-Si interface from  $6.3 \times 10^9$  to  $7.5 \times 10^9$  cm<sup>-2</sup>eV<sup>-1</sup> after 500s stress. The n<sup>+</sup>/p junction diode was not affected by this stress as observed from the capacitance- and current- voltage characteristics. The stress contributed to a decrease in the open-circuit voltage (V<sub>oc</sub>) while short-circuit current (I<sub>sc</sub>) remained unaffected. The conversion efficiency decreased by ~ 4.13% after 500s stress due to excess interface traps that contribute to recombination at the SiN<sub>x</sub>/n<sup>+</sup>-Si interface. Therefore, a degradation in the SiN:H/n<sup>+</sup>-Si interface can significantly deteriorate the solar cell performance.

## CHAPTER 6

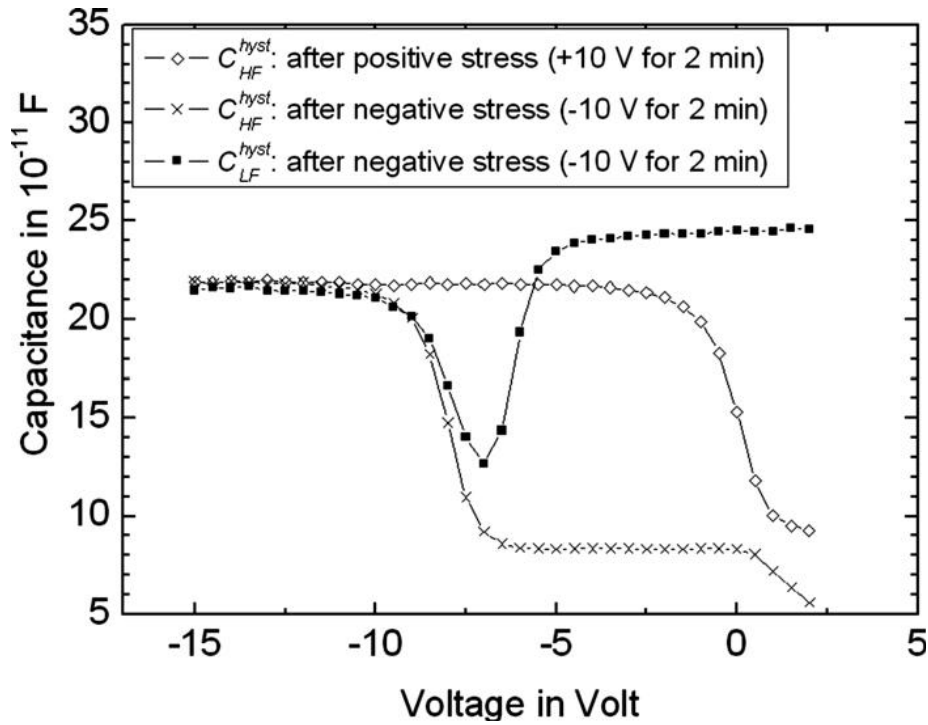
### CONSTANT VOLTAGE ILLUMINATION STRESS DEGRADATION

#### 6.1 Introduction

In constant voltage illumination stress (CVIS) study, a positive bias is applied to the Cu electrode of the  $\text{Cu/SiN}_x/\text{n}^+$  MOS capacitor under 1 sun light illumination condition whereas, in constant voltage stress (CVS) study, a positive bias is applied to the Cu terminal of the capacitor in dark condition as was performed in the previous Chapter (Chapter 5). Under light illumination conditions, electron-hole pairs are generated in the  $\text{n}^+$  layer. When a positive bias is applied to the gate terminal (Cu) of the MOS capacitor, electrons will move towards the interface and will break the Si-H bonds creating more number of silicon dangling bonds and hence generating more interface trap states at the  $\text{SiN}_x/\text{n}^+$  interface of the multilayered Si solar cell device. The degradation caused by CVIS is higher in comparison to that of CVS as more electron carriers flow towards the interface.

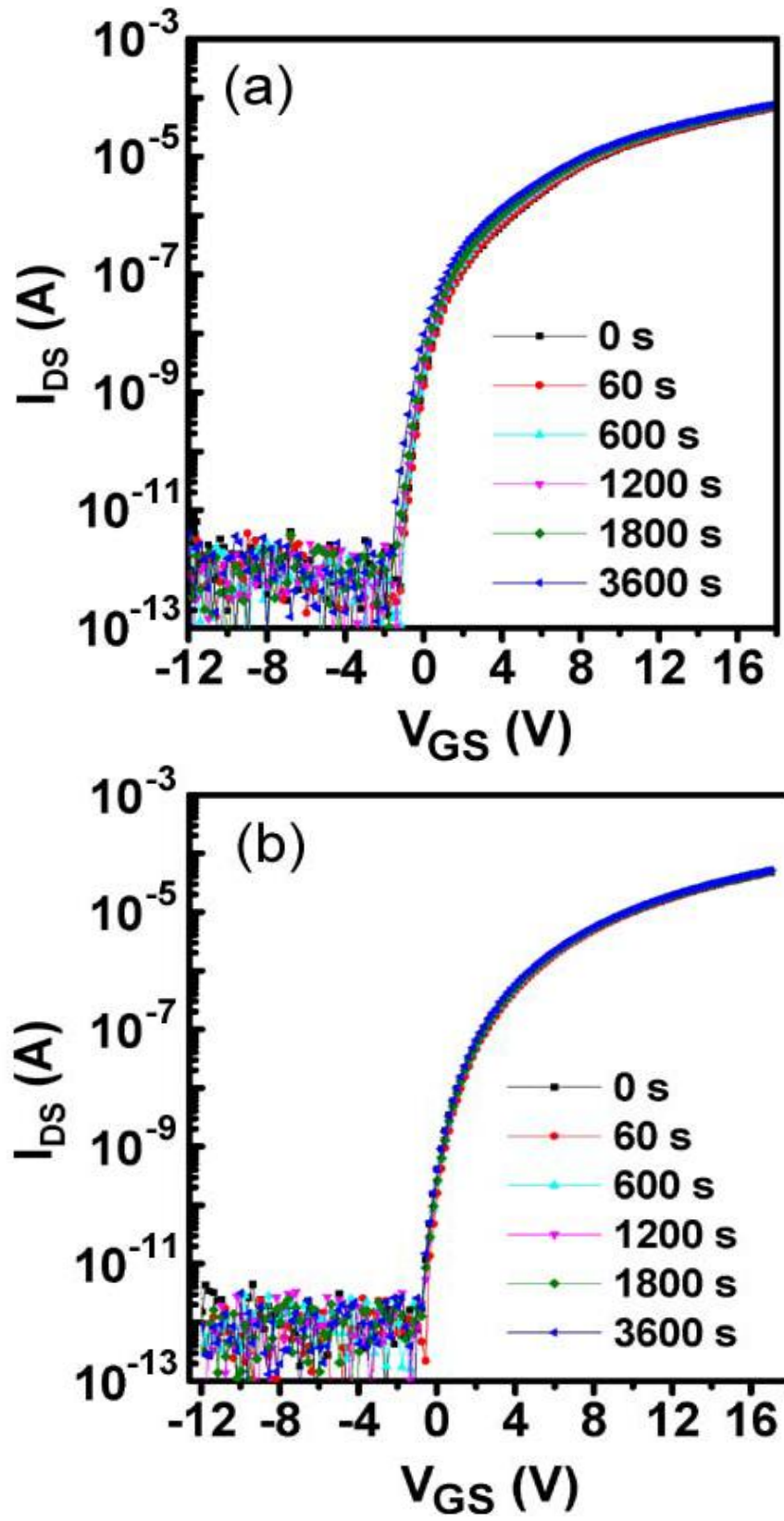
## 6.2 Background

Figure 6.1 shows the effect of both positive and negative voltage stress at 10V for 2 min on the C-V characteristics of SiN<sub>x</sub> dielectric deposited on p-type Si substrate. It is observed that there is a shift in the C-V plots.<sup>17</sup> This implies that there is degradation at the SiN<sub>x</sub>/p-Si interface due to this constant voltage stress.

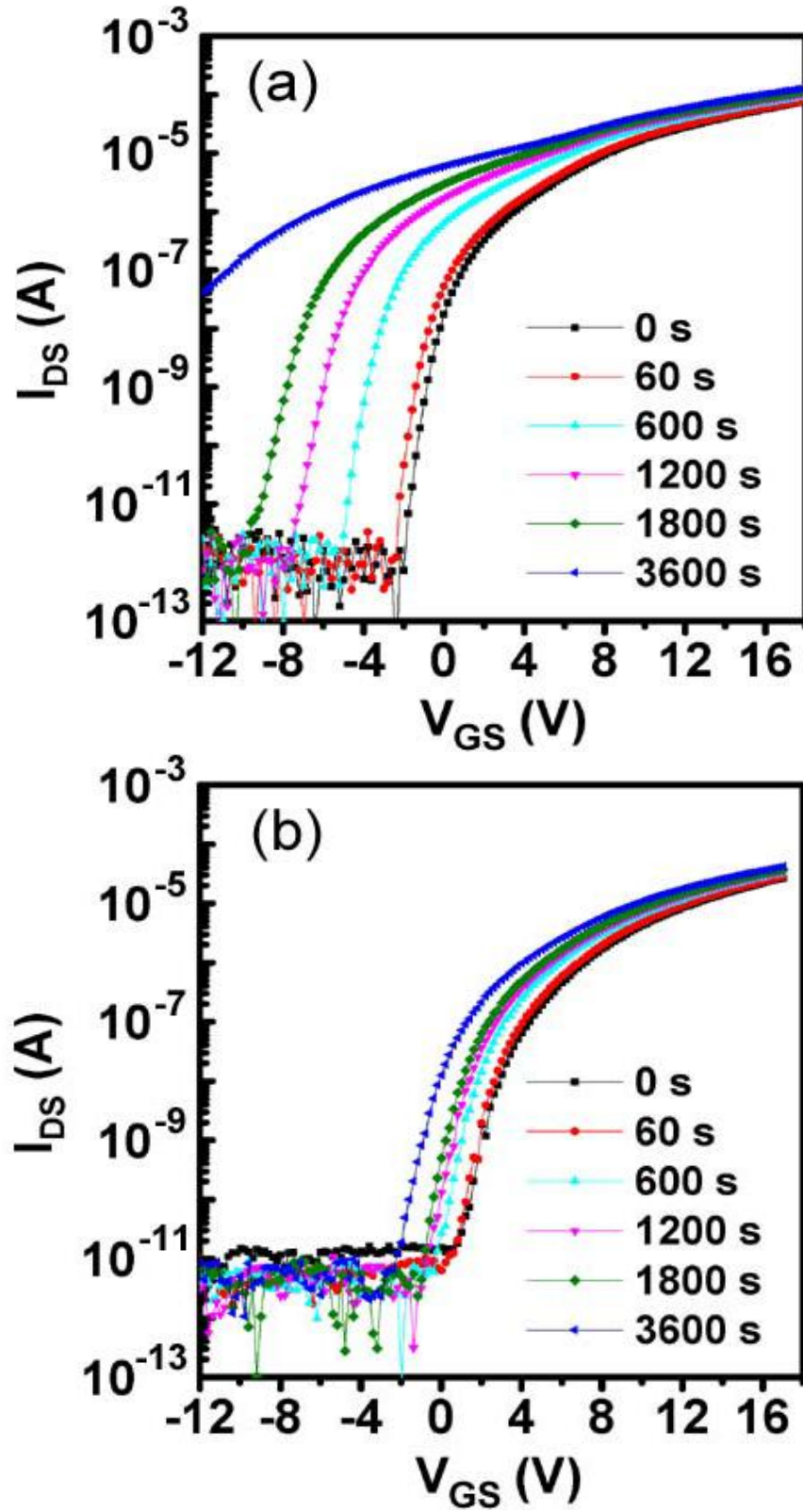


**Figure 6.1** HF and LF C-V characteristics of a SiN<sub>x</sub> layer on p-type Si after different constant voltage stress condition.<sup>17</sup>

Figures 6.2(a) and (b) show the transfer characteristics of thin film transistors (TFT) under negative bias stress (NBS) for different stress times in dark condition with SiN<sub>x</sub> and TiO<sub>2</sub>/SiN<sub>x</sub> gate dielectrics, respectively. It is observed that, TFT with SiN<sub>x</sub> dielectric, has more degradation in threshold voltage ( $V_{th}$ ) compared to TiO<sub>2</sub>/SiN<sub>x</sub> dielectric.



**Figure 6.2** Transfer characteristics of TFT with  $\text{SiN}_x$  (a) and  $\text{TiO}_2/\text{SiN}_x$  (b) with constant voltage stress under dark conditions.<sup>18</sup>



**Figure 6.3** Transfer characteristics of TFT with  $\text{SiN}_x$  (a) and  $\text{TiO}_2/\text{SiN}_x$  (b) with constant voltage stress under light illumination conditions.<sup>18</sup>



Figures 6.3(a) and (b) depict the transfer characteristics for TFT with  $\text{SiN}_x$  and  $\text{TiO}_2/\text{SiN}_x$  gate dielectrics, respectively, under negative bias stress in light illumination condition. It is seen that the degradation in threshold voltage ( $V_{th}$ ) is more for TFTs having  $\text{SiN}_x$  gate dielectric. This degradation is attributed to the injection of photo-induced hole carriers into the bulk region of the  $\text{SiN}_x$  gate dielectric.<sup>18</sup>

In this work, the degradation of  $\text{Cu}/\text{SiN}_x/\text{n}^+$  MOS capacitor under constant voltage stressing in both dark and light illumination conditions is studied and its impact on the Si solar cell performance parameters is presented.

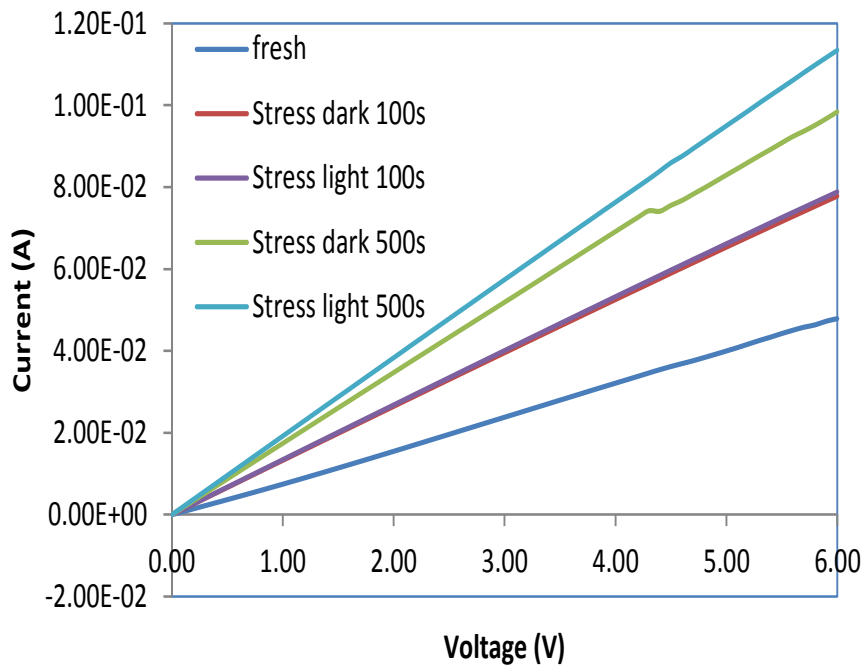
### 6.3 Experimental

In this study, a positive bias (+10 V) is applied to the gate terminal (Cu) of the  $\text{Cu}/\text{SiN}_x/\text{n}^+$  MOS capacitor under both dark (CVS) and 1 Sun light illumination condition (CVIS). The I-V measurements are taken for the MOS capacitor after constant voltage stressing in both light and dark conditions for different time intervals. Also, I-t characteristics are taken for different stress times for both light and dark conditions. The C-V and G-V characteristics of the MOS capacitor are taken after different stress times. The dark I-V, light I-V, and C-V (at 10 kHz) for p-n<sup>+</sup> junction diode are also taken.

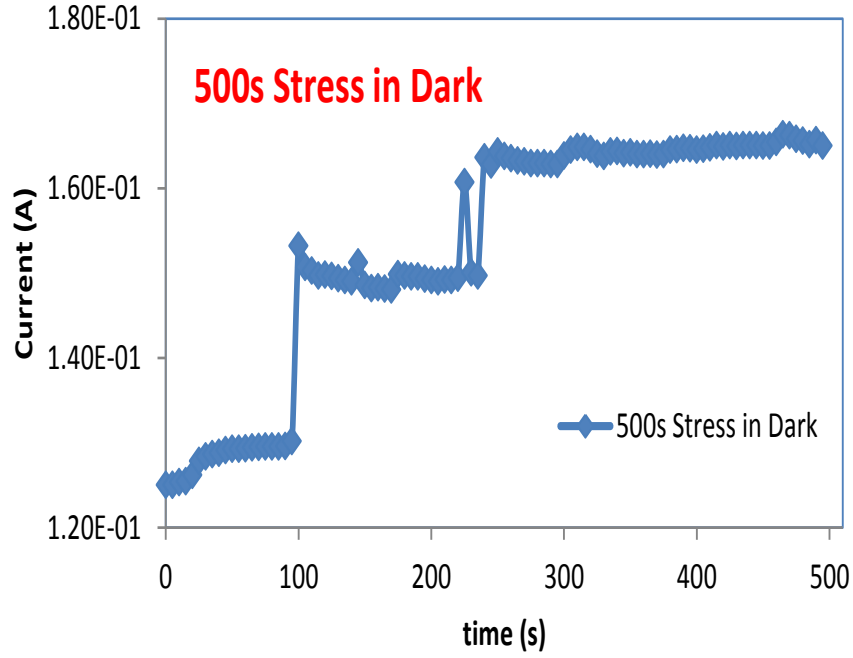
### 6.4 Results and Discussion

Figure 6.4 shows the I-V characteristics of  $\text{Cu}/\text{SiN}_x/\text{n}^+$  MOS capacitor for fresh devices as well as stressed devices in both dark and illumination conditions for different stress times. It is observed that the leakage current increases as the stress time increases. Also, it

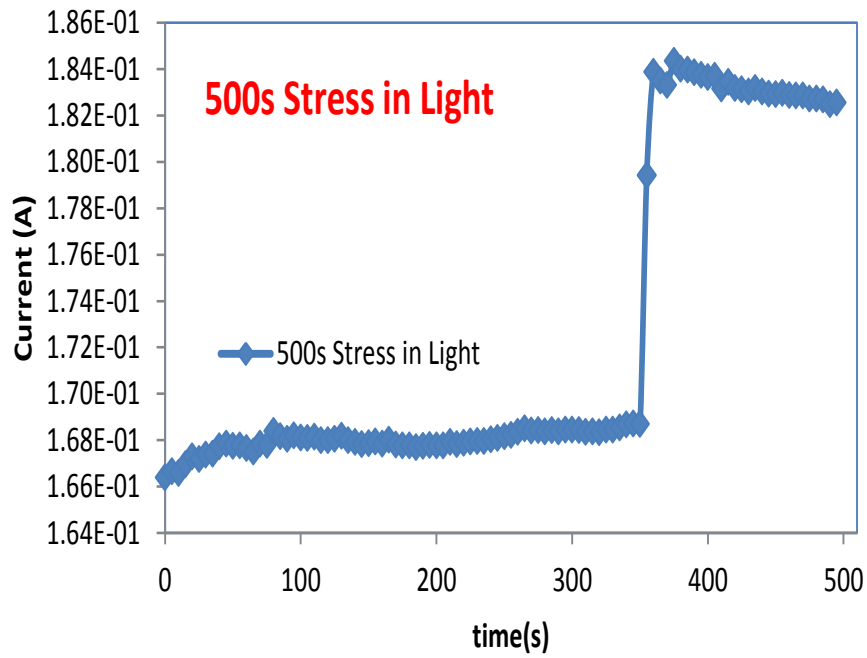
is seen that the leakage current for devices, stressed in illumination condition, is higher compared to that of devices stressed in dark condition. Figure 6.5 shows the variation of leakage current with stress time in dark condition. It is observed that the leakage current increases with the increase in stress time which is due to the increase of interface trap density with stress time. From Figure 6.6, it is also seen that the leakage current increases with stress time under illumination condition. The leakage current, after CVIS, is higher than that of after CVS.



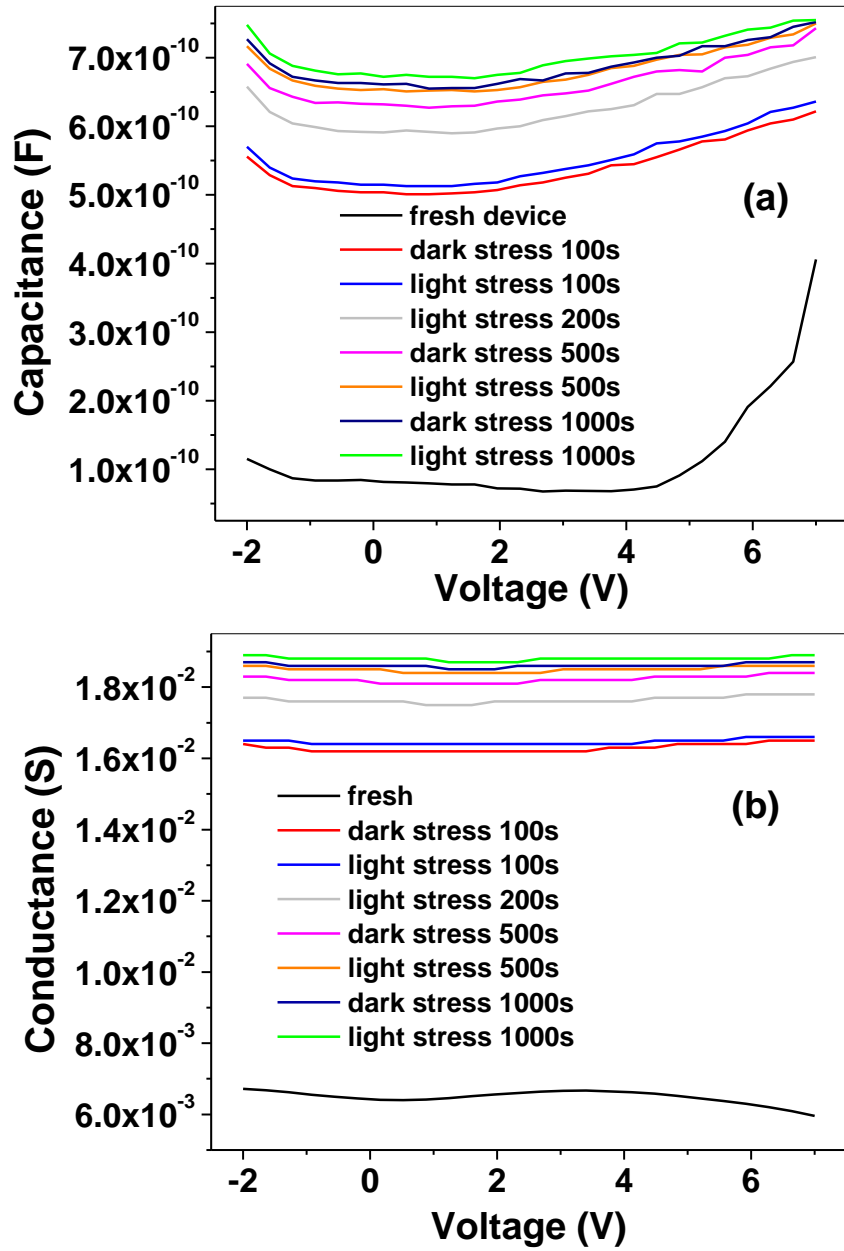
**Figure 6.4** I-V characteristics of Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor for different stress times after CVS at 10 V under dark and illumination conditions.



**Figure 6.5** I-t characteristics of Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor after CVS at 10 V under dark.



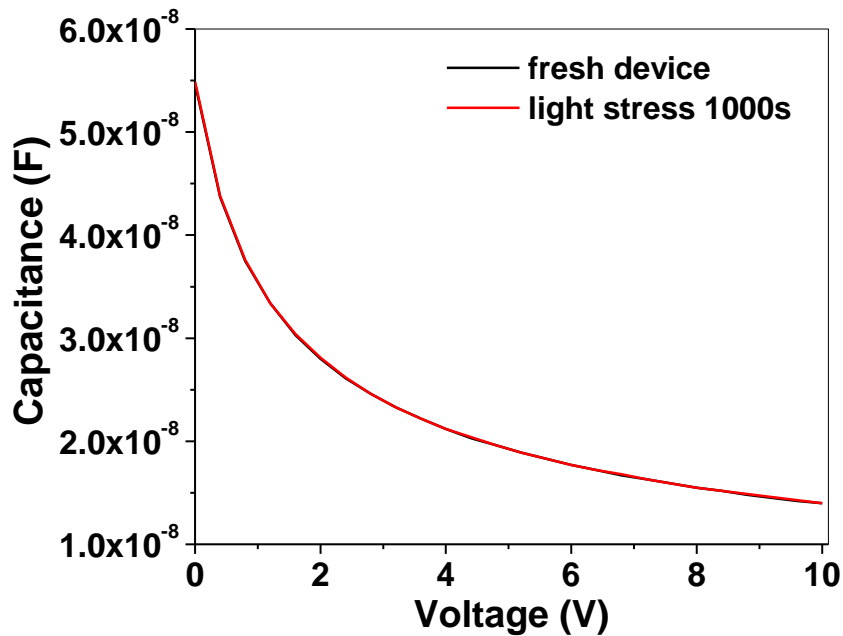
**Figure 6.6** I-t characteristics of Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor after CVS at 10 V under illumination.



**Figure 6.7** (a) C-V and (b) G-V characteristics at 10 kHz for different stress times for both dark and light stress.

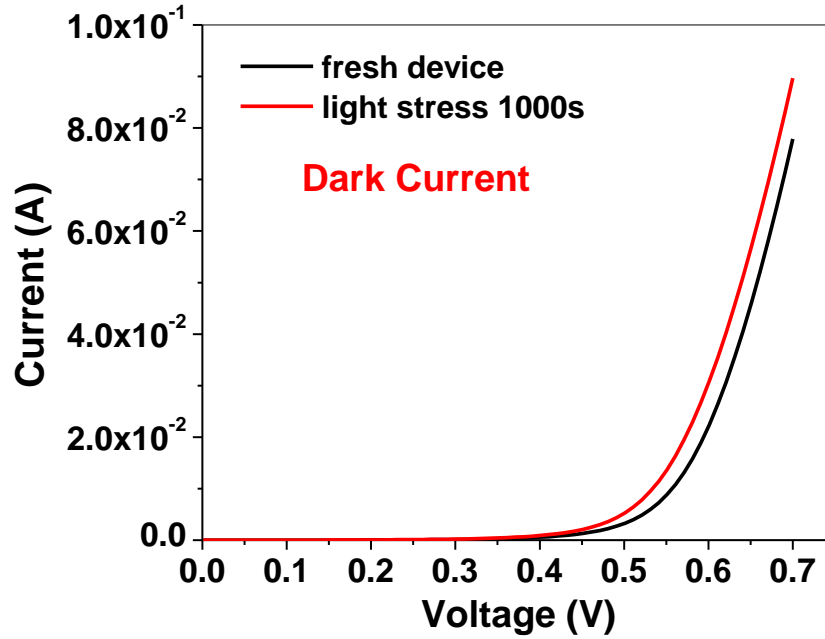
Figure 6.7 (a) and (b) show the C-V and G-V characteristics, respectively for Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor for different stress times at CVS of + 10 V under both dark and light illumination conditions. The observed increment in C-V and G-V characteristics

with stress times is due to the creation of more interface traps at the  $\text{SiN}_x/\text{n}^+\text{Si}$  interface. It is seen that both C-V and G-V increases for devices stressed under illumination condition compared to dark condition. The main effect of illumination on the C-V characteristics of a MOS capacitor is that the capacitance in the heavy inversion region approaches the low frequency value as the illumination intensity increases. The basic mechanism responsible for this effect is that, under illumination, generation of electron-hole pairs by photons occurs, which causes a decrease in the surface potential  $\psi_s$  under constant applied voltage.<sup>2</sup> This decrease of  $\psi_s$  results in a reduction of the width of the space-charge layer, with a corresponding increase of the capacitance. The same mechanism is also responsible for the increment in G-V characteristics.



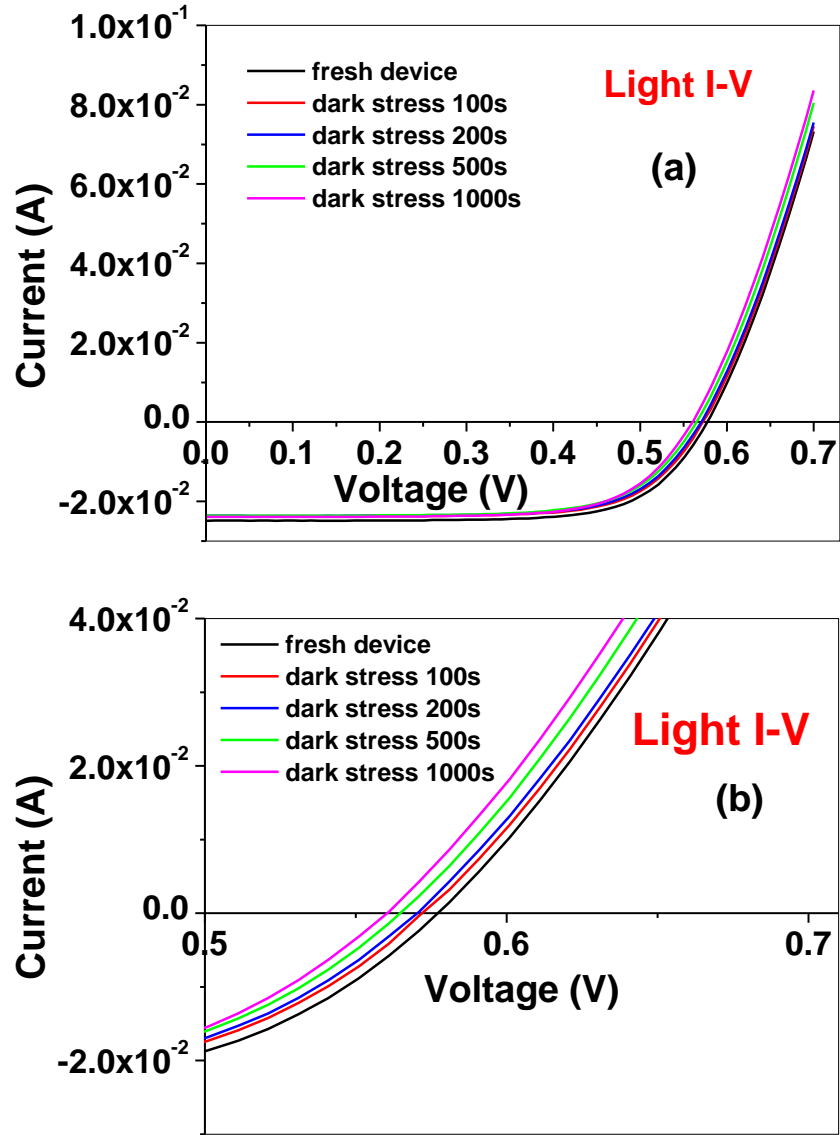
**Figure 6.8** C-V characteristics of  $\text{p-n}^+$  junction diode at 10 kHz for different stress.

Figure 6.8 shows the C-V characteristics of  $p-n^+$  junction for fresh devices as well as stressed device for 1000s stress time under illumination condition. It is observed that there is no shift in the C-V curves. This implies that there is no generation of any bulk traps at the depletion region.



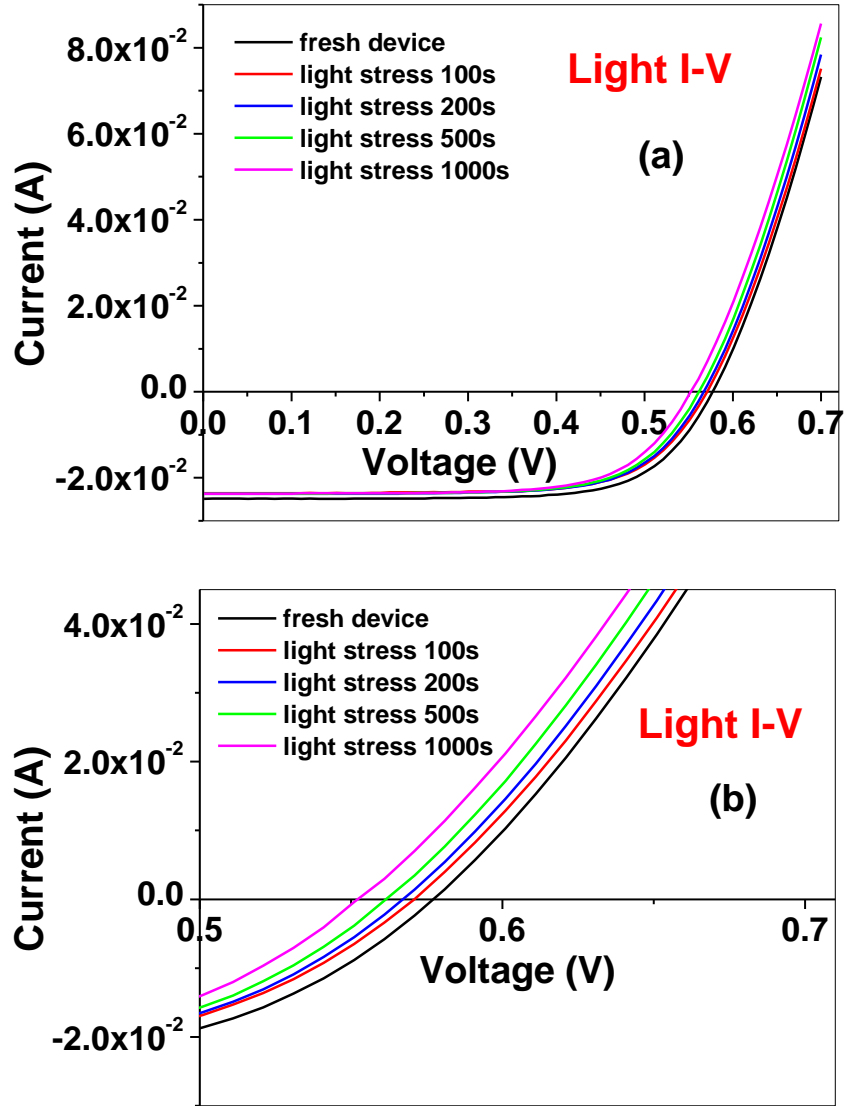
**Figure 6.9** Dark I-V characteristics of  $p-n^+$  junction diode for different stress.

Figure 6.9 shows the dark I-V characteristics of  $p-n^+$  junction diode for the fresh device and the stressed device under light illumination for 1000s stress time. It is observed that there is a shift in dark I-V plots. Thus, the degradation is more for CVS under illumination. This shift in dark I-V curves is absent for CVS under dark conditions as shown in Figure 5.4(a) in Chapter 5. Therefore, the degradation is more under illumination compared to that in dark condition.



**Figure 6.10** Light I-V characteristics of p-n<sup>+</sup> junction diode for different stress time under dark stress (a) and the enlarged version is shown in (b).

Figures 6.10 (a) and (b) show the light I-V characteristics of p-n<sup>+</sup> junction diode for CVS at 10 V under dark condition for different stress times. It is observed that there is shift in the light I-V plots with stress time. This degradation is due to the increase in interface trap density ( $D_{it}$ ) with stress time.



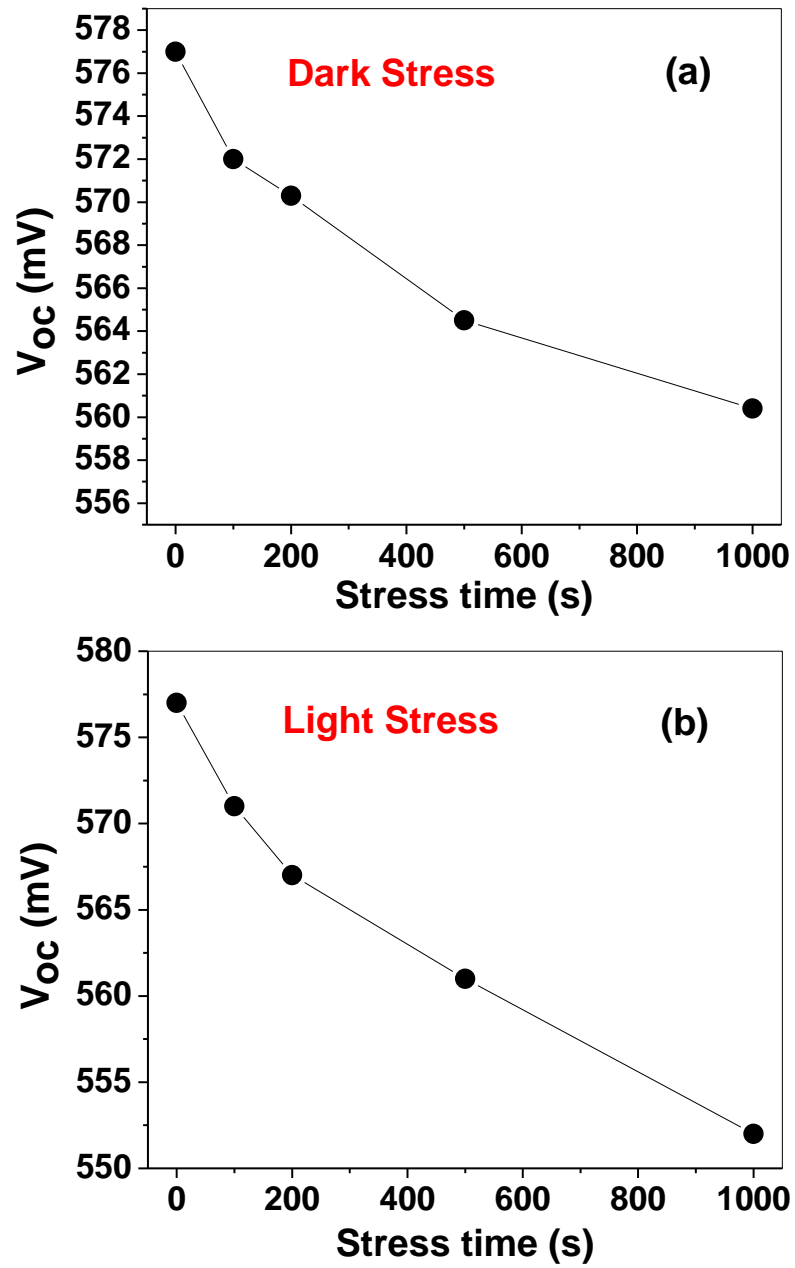
**Figure 6.11** Light I-V characteristics of p-n<sup>+</sup> junction diode for different stress time under light stress (a) and the enlarged version is shown in (b).

Figures 6.11 (a) and (b) show the light I-V characteristics of p-n<sup>+</sup> junction diode for CVS at + 10V for different stress times under illumination condition. It is observed that there is a shift in the I-V curve towards the left with the increase in stress time which is due to the increase in the interface trap density ( $D_{it}$ ) at the SiN<sub>x</sub>/n<sup>+</sup>Si interface. It is

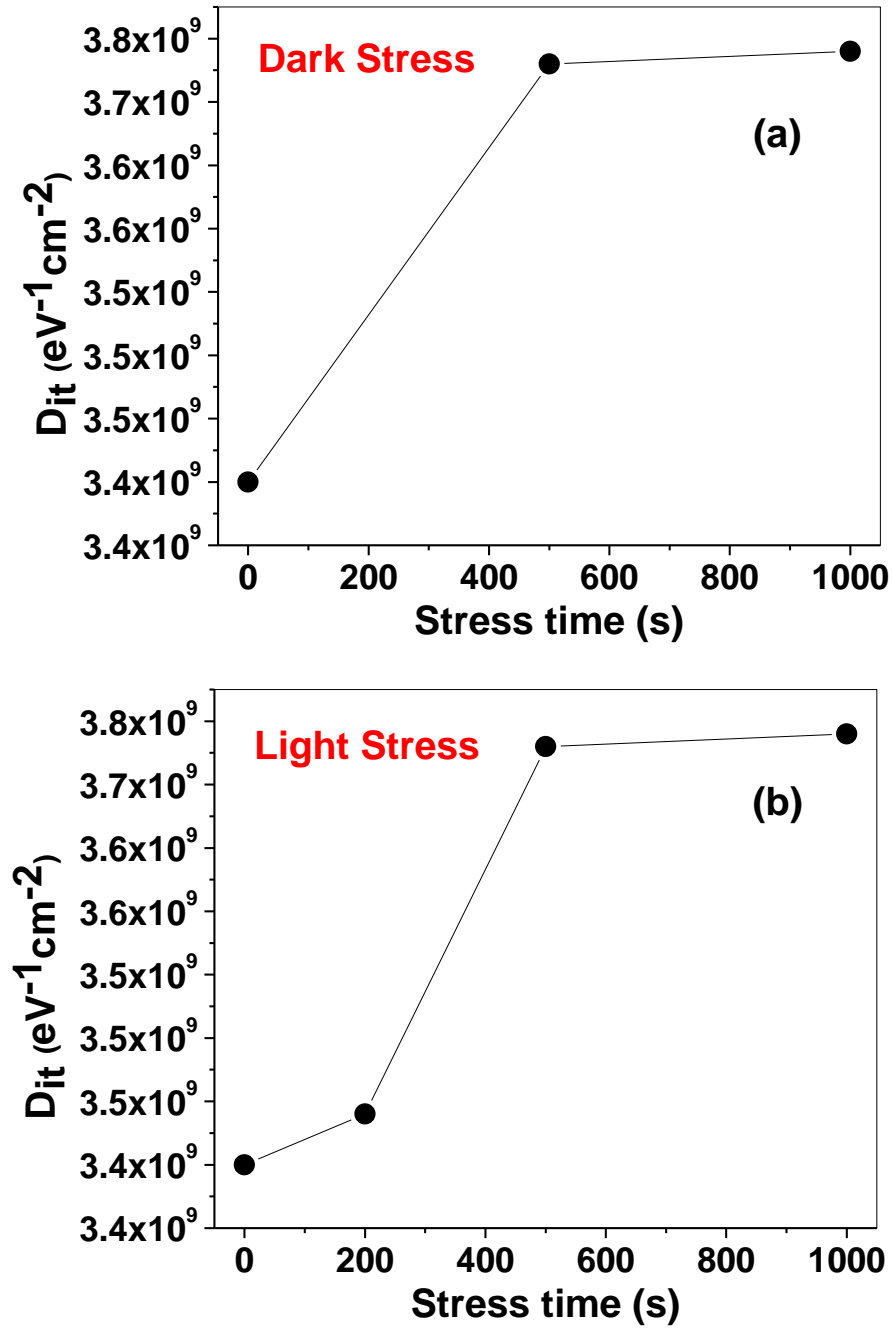


known that  $\text{SiN}_x$  is used as a gate insulator (GI) in thin film transistors (TFTs). The oxide TFTs are well known to be adversely affected by the bias illumination stress (BIS). In particular, the gate insulator (GI) material plays a critical role in determining the BIS instability. The gate-bias driven migration of photo-generated hole carriers and subsequent hole trapping or injection at the interface is responsible for this strong GI material-dependent negative bias illumination stress (NBIS) instability in TFTs.<sup>18</sup> In the positive constant voltage stress under light illumination, there is migration of photo-induced electron carriers and subsequent electron trapping or injection at the  $\text{SiN}_x/\text{n}^+$  interface, which is responsible for the enhanced shift of light I-V plots and, hence, more degradation under illumination compared to dark condition.<sup>19</sup> Thus, under illumination condition, increase in interface trap density ( $D_{it}$ ) and electron trapping at the interface take place.

Figures 6.12 (a) and (b) show the variation of open-circuit voltages ( $V_{oc}$ ) with stress time for both dark and light voltage stress conditions, respectively. It is observed that, in both dark and light conditions,  $V_{oc}$  decreases as the stress time increases. This degradation occurs because of the increment in interface trap density ( $D_{it}$ ). Also, it is seen that the  $V_{oc}$  value is more for constant voltage stress under dark compared to that under illumination condition. The enhanced degradation under illumination is due to both increase in  $D_{it}$  and electron trapping at the interface.



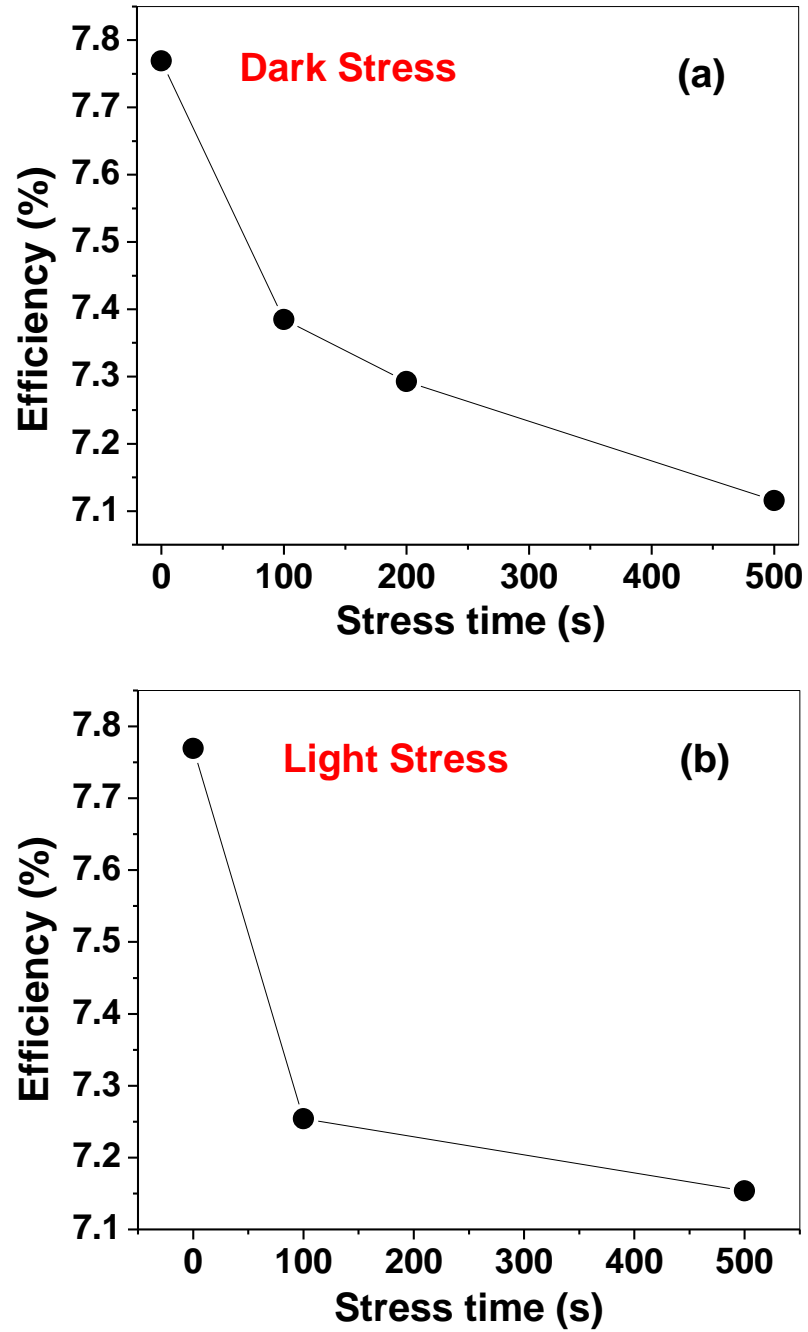
**Figure 6.12** Open-circuit voltage ( $V_{oc}$ ) vs. stress time under dark stress (a) and light stress (b).



**Figure 6.13** Interface trap density ( $D_{it}$ ) vs. stress time for dark stress (a) and light stress (b).

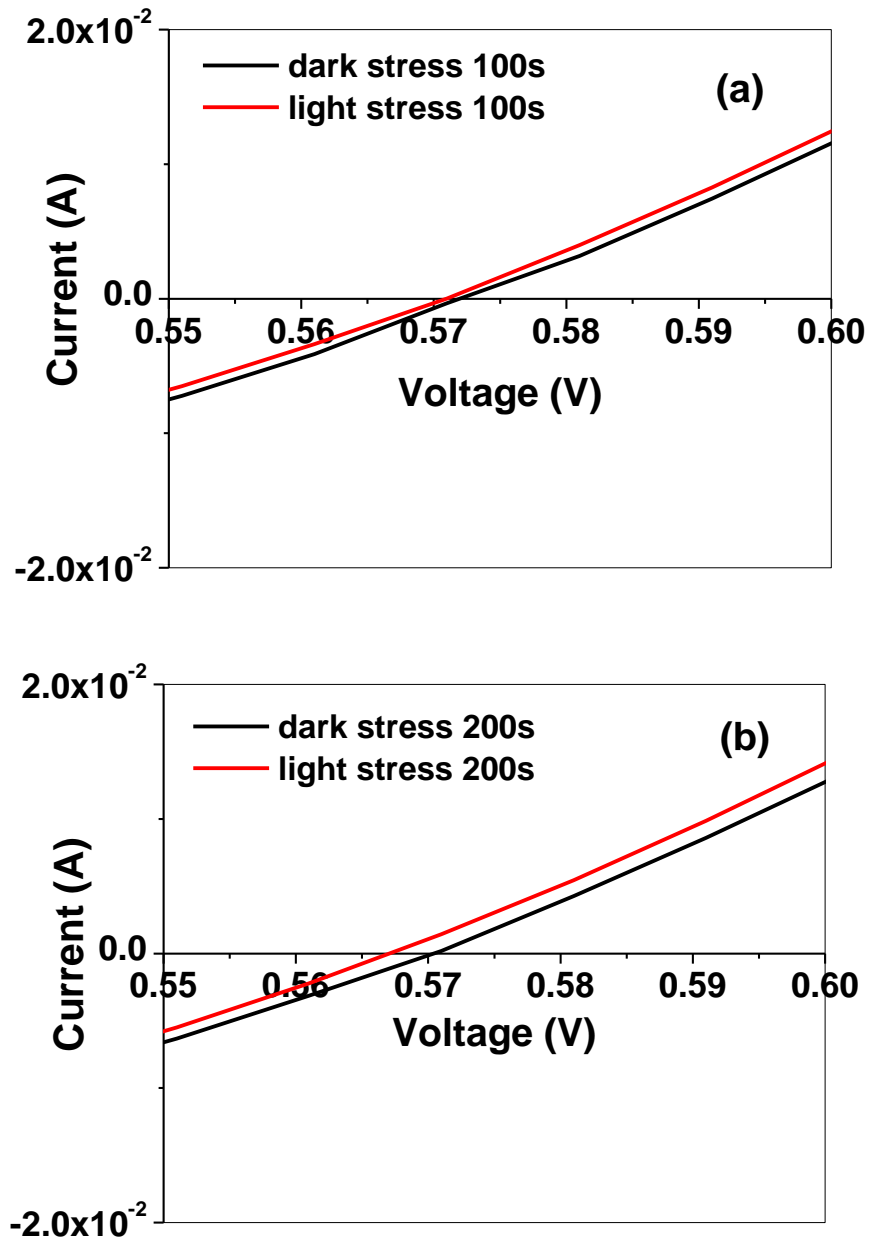
The variation in interface trap density ( $D_{it}$ ) with stress time is shown for both dark and illumination conditions in Figures 6.13 (a) and (b), respectively. It is observed that

$D_{it}$  increases with stress time in both conditions due to creation of more Si dangling bonds.

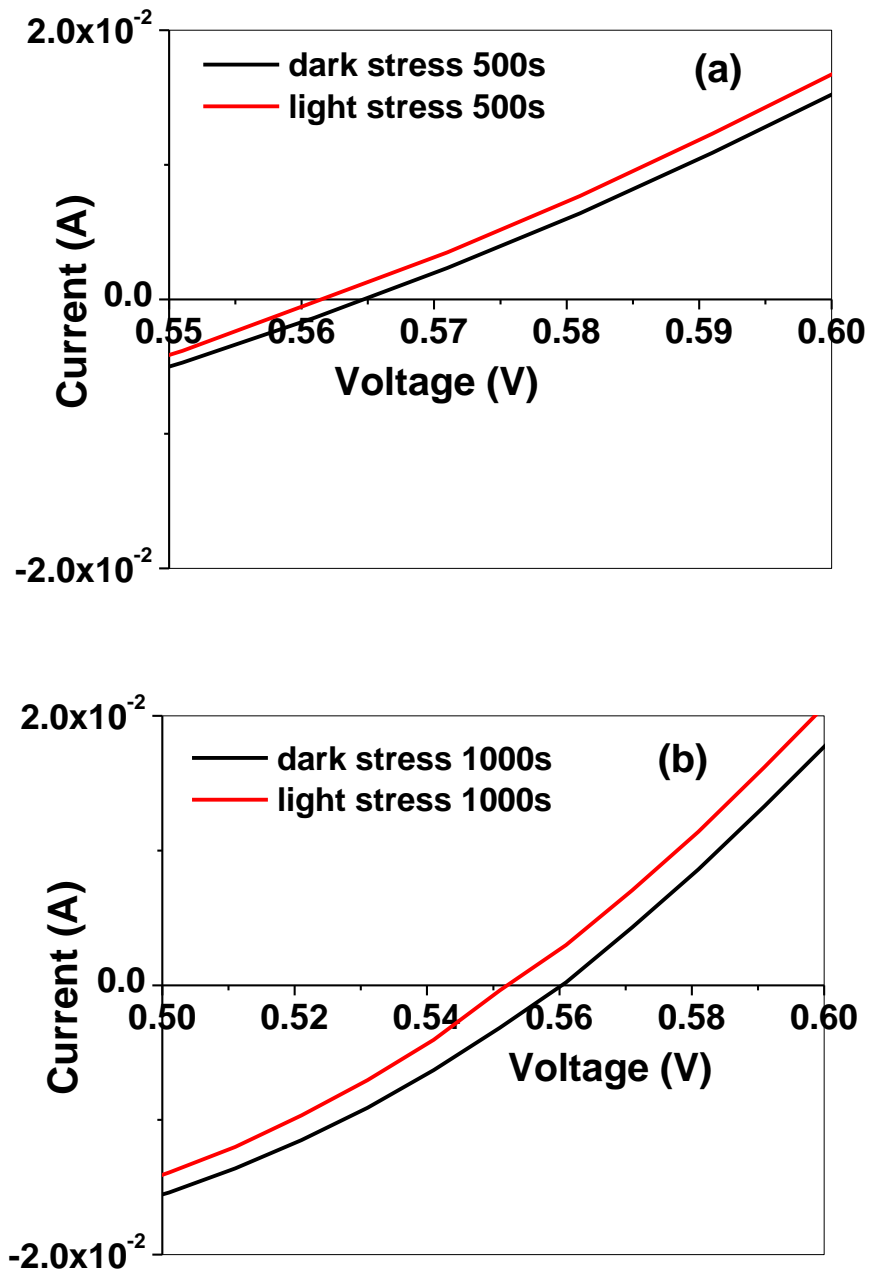


**Figure 6.14** Conversion efficiency ( $\eta$ ) vs. stress time for dark stress (a) and light stress (b).

Figures 6.14 (a) and (b) show the variation of conversion efficiency with stress time for CVS under dark and light illumination. It is observed that, in both cases, the efficiency decreases with stress time due to the creation of more interface traps and, hence, increase in  $D_{it}$ .



**Figure 6.15** Comparison of enlarged view of light I-V characteristics for dark and light stress conditions for 100s (a) and 200s (b).



**Figure 6.16** Comparison of enlarged view of light I-V characteristics for dark and light stress conditions for 500s (a) and 1000s (b).

Figures 6.15 (a) and (b) show the comparison of light I-V under dark and light stress for 100s (a) and 200s (b) stress time, respectively. It is clearly observed that the degradation is more when the device is stressed under illumination condition compared to dark condition. Similar behavior is also seen for 500s and 1000s stress times for both dark and light conditions as shown in Figure 6.16 (a) and (b), respectively. The observed enhanced degradation under illumination compared to dark condition is due to increase in  $D_{it}$  as well as electron trapping at the  $\text{SiN}_x/\text{n}^+$  interface.

## 6.5 Conclusions

Constant voltage stress under dark and illumination has been carried out at +10V on  $\text{Cu/SiN}_x/\text{n}^+$  MOS capacitors. It is observed that the leakage current as well as both C-V and G-V increase with stress time. Therefore, the interface trap density ( $D_{it}$ ) increases. The solar cell performance parameters such as  $V_{oc}$  and conversion efficiency decrease with stress time for CVS at 10V under both dark and light conditions due to the increase in  $D_{it}$ .

## CHAPTER 7

### CONCLUSIONS

In summary, a constant voltage stress (CVS) of +10 V is applied for different stress times to the Cu/SiN<sub>x</sub>/n<sup>+</sup>-Si MOS capacitor in a multicrystalline Si solar cell to investigate the effects of SiN<sub>x</sub>/n<sup>+</sup>-Si interface degradation on Si solar cell performance characteristics. Significant shifts in I-V, C-V, and G-V characteristics of SiN<sub>x</sub> MOS capacitor were observed demonstrating an increase in interface trap density across the SiN<sub>x</sub>/n<sup>+</sup>-Si interface from  $6.3 \times 10^9$  to  $7.5 \times 10^9 \text{ cm}^{-2}\text{eV}^{-1}$  after 500s stress. The n<sup>+</sup>/p junction diode was not affected by this stress as observed from the capacitance - voltage and current - voltage characteristics. The stress contributed to a decrease in open-circuit voltage ( $V_{oc}$ ) from 570 to 550 mV while short-circuit current ( $I_{sc}$ ) remained unaffected. The conversion efficiency decreased by  $\sim 4.13\%$  after 500s stress due to excess interface trap related recombination at the SiN<sub>x</sub>/n<sup>+</sup>-Si interface. Therefore, a degradation of the SiN:H/n<sup>+</sup>-Si interface can significantly deteriorate the solar cell performance.

A constant voltage stress, under both dark and light illumination conditions, has been applied at +10V on Cu/SiN<sub>x</sub>/n<sup>+</sup> MOS capacitor in a multicrystalline Si solar cell. It is observed that the leakage current as well as both C-V and G-V of MOS capacitor increase with stress time for dark and illumination. Therefore, the interface trap density, ( $D_{it}$ ), increases with stress time. The solar cell parameters, such as  $V_{oc}$  and conversion efficiency ( $\eta$ ), decrease with stress time under both dark and illumination conditions due to the increase in  $D_{it}$ . The degradation in cell parameters is more when the MOS capacitor



is voltage stressed under illumination compared to dark condition due to the increase in  $D_{it}$  as well as photo-induced electrons trapped at the  $\text{SiN}_x/\text{n}^+\text{Si}$  interface.

After 5 hrs of light soaking of the mono-crystalline Si solar cell, it is observed that there is an increase in both C-V and G-V characteristics of the entire solar cell compared to the fresh device. Thus, there is an increase in interface trap density, ( $D_{it}$ ), at the  $\text{SiN}_x/\text{n}^+$  interface after soaking. Therefore, this increase in  $D_{it}$  affects the Si solar cell parameters after light soaking.

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